Power LSI series for Digital Camera and Digital Video Camera

4CH Internal Power MOSFET System Switching Regulator

BD9866GUL

●**Outline**

BD9866GUL is a 4ch DC/DC converter IC composed of Buck converter 3-channels and Buck-Boost converter 1-channel.Including power MOSFET of all channels reduces the number of peripheral devices. Each channel is controlled individually, that enables to reduce power consumption of not working channel.

●**Features**

1) Includes Buck converter (CH1, 2 and 4), and Buck-Boost converter (CH3), total 4 channels included.
2) Includes Power MOSFET for all channels.
3) Includes Over Current Protection (OCP) for all channels.
4) Includes Short Circuit Protection (SCP.)
5) Includes Undervoltage Lock Out (UVLO.)
6) Includes Thermal Shut Down (TSD.)
7) Includes Power Good(PG)
8) External synchronous oscillation
9) Each channel can be turn on/off individually.
10) Contains internal compensation for all channels.
11) Operation frequency of 1MHz.

●**Package**

WLCSP(3.75mm×3.75mm)

●**Use**

For digital single-lens reflex camera, digital video camera.

●**Key specifications**

- Input voltage range : 4.0V to 14.0V
- Output voltage
  - CH1 reference voltage: 0.6V±1.67% (typ.)
  - CH2 reference voltage: 0.8V±1.25% (typ.)
  - CH3 reference voltage: 0.8V±1.25% (typ.)
  - CH4 reference voltage: 0.8V±1.25% (typ.)
- Load current
  - CH1 load current: 3.0A(max)
  - CH2 load current: 2.0A(max)
  - CH3 load current: 1.5A(max)
  - CH4 load current: 3.0A(max)
- Frequency: 1MHz(typ.)

●**Function block diagram**

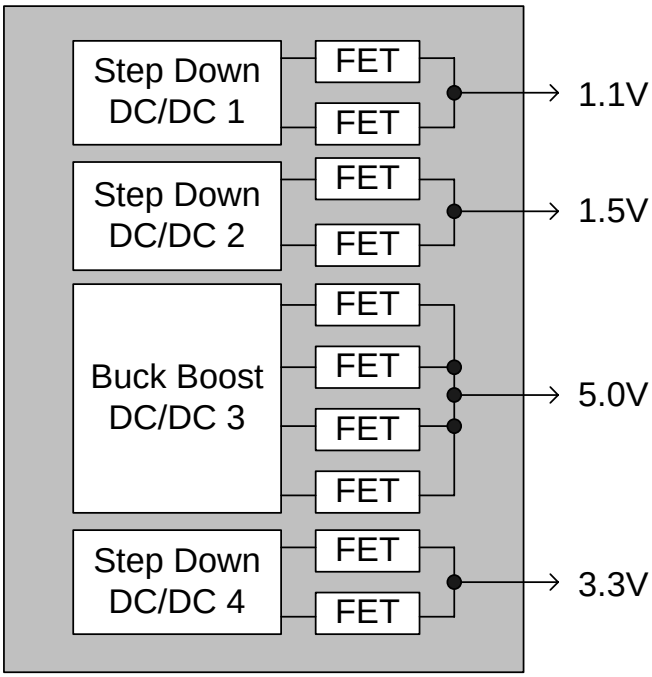

Figure. 1 Function block diagram

●**Pin assignment(Bottom View)**

G	PVCC1	PVCC1	VREGD	PVCC	GND	VCC	PVCC4
F	Lx1	CH1G	INV1	VREGB	VREGA	RT	PVCC4
E	Lx1	CH2G	SYNC	INV3	INV4	Lx4	Lx4
D	PGND1	PGND1	CTL2	INV2	RTSS	PGND4	PGND4
C	PGND2	PGND2	1pin POST	CTL1	CTL4	CTL3	SEL
B	Lx2	Lx2	PGND	SCP	PG	Lx32	VO3
A	PVCC2	PVCC2	PVCC3	Lx31	PGND3	PGND3	Lx32
	1	2	3	4	5	6	7

Figure.2 Pin assignment

●**Pin description**

PINno	Symbol	I/O	Description
G6	VCC	-	Input supply voltage
G4	PVCC	-	Input supply voltage of internal regulator for driver
B3	PGND	-	Ground terminal
G1,G2,A1,A2, A3,F7,G7	PVCC1,2,3,4	-	Driver input supply voltage terminal.
D1,D2,C1,C2, A5,A6,D6,D7	PGND1,2,3,4	-	Ground for internal FET
G5	GND	-	Ground
G3	VREGD	O	Output terminal of 3.5V regulator for lowside driver
F5	VREGA	O	Output terminal of 3.5V regulator for internal reference voltage
F4	VREGB	O	Output terminal of PVCC – 3.5V regulator for highside driver
B7	Vo3	O	Output voltage terminal for CH3
E1,F1,B1,B2, E6,E7	Lx1,2,4	O	Inductor connecting terminal
A4	Lx31	O	CH3 input side inductor connecting terminal
A7,B6	Lx32	O	CH3 output side inductor connecting terminal
F3,D4,E4,E5	INV1,2,3,4	I	Error amplifier inverted input terminal
E3	SYNC	I	External oscillator input terminal
F6	RT	-	Oscillator frequency adjustment terminal with external resistor
B4	SCP	-	SCP delay time setting terminal with external capacitor
C4,D3,C6,C5	CTL1,2,3,4	I	ON/OFF control terminal
B5	PG	O	Power good signal output terminal at SCP
F2,E2	CH1,2G	O	CH1,2 power good signal output terminal
D5	RTSS	O	RT voltage setting terminal
C7	SEL	I	CH2,4 mode select terminal

●**block diagram**

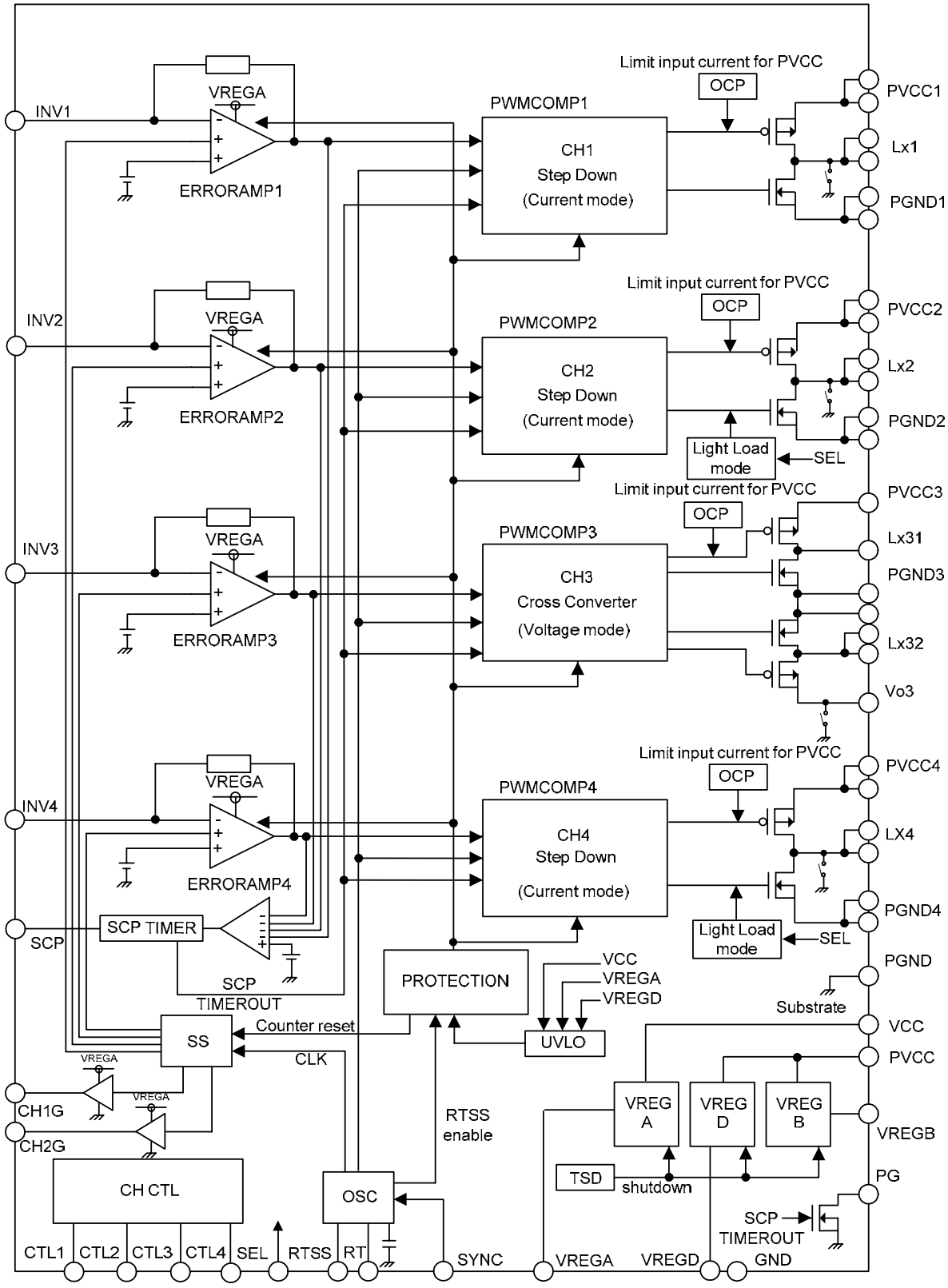

Figure. 3 block diagram

●**Absolute Maximum Ratings**

Parameter	Symbol	Limits	Units
Maximum Power Supply Voltage	VCC, PVCC, PVCC1,2,3,4	-0.3 to 15	V
Maximum Input Current	IPVCC1,4	3.5	A
	IPVCC2,3	2.5	A
Maximum Input Voltage	VREGA, VREGD, PVCC1,2,3,4-VREGB	-0.3 to 7	V
	Lx1, Lx2, Lx31, Lx4	-0.3 to 15	V
	Lx32, Vo3	-0.3 to 10.5	V
	PG	-0.3 to 15	V
	CH1,2G	-0.3 to 7	V
	CTL1,2,3,4	-0.3 to 15	V
	SEL	-0.3 to 15	V
	SYNC	-0.3 to 15	V
Power Dissipation	Pd	1.25(*1)	W
Operating Temperature	Topr	-25 to +85	℃
Storage Temperature	Tstg	-55 to +125	℃
Junction Temperature	Tjmax	125	℃

(1*)when mounted on a 50mm×50mm×1.75mm glass epoxy 8layer PCB at Ta=25℃(Derate by 12.5mW/℃ above 25℃)

●**Recommended Operating Conditions**

Parameter	Symbol	Limits			Units	Conditions
		Min	Typ	Max		
Power Supply Voltage	VCC,PVCC	4.0	6.0	14	V	
VREGA,VREGD Output Capacitor	CVREGA,D	0.47	1.0	2.2	µF	
VREGB Output Capacitor	CVREGB	0.47	1.0	2.2	µF	Connect to PVCC
Capacitor Connected to SCP	CSCP	0.001	―	2.2	µF	
Oscillator Frequency	FOSC	0.6	1.0	1.5	MHz	
OSC Timing Resistor	RT	47	82	120	kΩ	1MHz by connecting 82kΩ
Capacitor Connected to RTSS	CRTSS	1000	10000	―	pF	
H Level of SYNC Input voltage	VSYNCH	3.0	-	VCC	V	
L Level of SYNC Input voltage	VSYNCL	-0.3	-	0.5	V	
Duty of SYNC Input	DSYNC	40	50	60	%	
Output voltage range of CH3	VVOUT3	4.0	―	10	V	
Output Current of CH1	IOUTCH1	―	―	3(*3)	A	1.1V Output
Output Current of CH2	IOUTCH2	―	―	2(*3)	A	1.5V Output
Output Current of CH3	IOUTCH3	―	―	1.5(*3)	A	5.0V Output
Output Current of CH4	IOUTCH4	―	―	3(*3)	A	3.3V Output

(*) Please connect capacitor to I/O(VCC, PVCC, VREG) so that IC can be operated safety.

(*3) Please make a power design total loss of IC not to exceed the power dissipation.

●**Over Current Protection**

Parameter	Symbol	Limits			Units	Conditions
		Min	Typ	Max		
CH1 PVCC1 OCP Current	IOCP1	3.2	-	-	A	
CH2 PVCC2 OCP Current	IOCP2	2.2	-	-	A	
CH3 PVCC3 OCP Curernt	IOCP3	3.0	-	-	A	
CH4 PVCC4 OCP Current	IOCP4	3.2	-	-	A	

●**Electrical Characteristics（Ta=25℃, VCC=PVCC=6V, RT=82kΩ, CTL1-4=3V, unless otherwise noted)**

Parameter	Symbol	Limits			Units	Conditions
		Min	Typ	Max		
【Internal Regulator】						
Regulator output voltage for internal analog circuit	VREGA	3.3	3.5	3.7	V	IVREGA=-1mA
Regulator output voltage for bias voltage of Highside FET	VREGB	VCC-3.7	VCC-3.5	VCC-3.3	V	IVREGB=+1mA
Regulator output voltage for bias voltage of Lowside FET	VREGD	3.3	3.5	3.7	V	IVREGD=-1mA
【Under Voltage Lock Out】						
Threshold voltage of VCC undervoltage lock out	VSTD1	3.2	3.4	3.6	V	VCC terminal voltage monitor
Hysteresis voltage of VCC undervoltage lock out	VHYS1	—	0.1	0.2	V	VCC terminal voltage monitor
Threshold voltage of VREG undervoltage lock out	VSTD2	2.8	3.0	3.2	V	VREGA,VREGD terminals voltage monitor
Hysteresis voltage of VREG undervoltage lock out	VHYS2	—	0.1	0.2	V	VREGA,VREGD terminals voltage monitor
【Short Circuit Protection】						
SCP terminal output current	ISCP	2.5	5.0	7.5	μA	VSCP=0.1V
SCP terminal detect voltage	VTSC	0.45	0.50	0.55	V	
SCP terminal stand-by voltage	VSSC	—	10	100	mV	
【Oscillator】						
Oscillator frequency of DC/DC converter	FOSC	0.9	1.0	1.1	MHz	RT=82kΩ
Max duty Lx1,Lx2,Lx4	DMAX1,2,4	-	-	100	%	VSCP=0V (*4), Lx1,Lx2,Lx4 High Duty
Max duty Lx31	DMAX31	-	-	100	%	Lx31 High Duty
Max duty Lx32	DMAX32	74	80	86	%	Lx32 Low Duty
RTSS terminal stand-by voltage	RTSSF	-	1	20	mV	CTL1-4=0V
RTSS terminal input current	IRTSSI	-7	-5	-3	μA	
RTSS terminal output current	IRTSSO	3	5	7	μA	
【Error Amplifier】						
INV1-4 terminal input bias current	IINV1,2,3,4	-50	0	50	nA	INV=2.0V
INV1 terminal threshold voltage	VINV1	0.590	0.600	0.610	V	
INV2-4 terminal threshold voltage	VINV2,3,4	0.790	0.800	0.810	V	
【Soft Start】						
CH1 Soft start time	TSS1	0.7	1.4	2.1	msec	
CH2,3,4 Soft start time	TSS2,3,4	0.95	1.9	2.85	msec	

(*4) SCP circuit starts to charge when operated 100% Duty, therefore it is possible to use 100% Duty only while SCP voltage doesn't reach to 0.5V.

●**Electrical Characteristics**（**Ta=25℃, VCC=PVCC=6V, RT=82kΩ, CTL1-4=3V, unless otherwise noted)**

Parameter	Symbol	Limits			Units	Conditions
		Min	Typ	Max		
【Driver】						
Lx1 Highside SW on resistance	RON1P	-	180	300	mΩ	ILx1=-50mA
Lx1 Lowside SW on resistane	RON1N	-	75	130	mΩ	ILx1=+50mA
Lx2 Highside SW on resistance	RON2P	-	190	305	mΩ	ILx2=-50mA
Lx2 Lowside SW on resistance	RON2N	-	100	160	mΩ	ILx2=+50mA
Lx31 Highside SW on resistance	RON31P	-	190	305	mΩ	ILx31=-50mA
Lx31 Lowside SW on resistance	RON31N	-	115	185	mΩ	ILx31=+50mA
Lx32 Highside SW on resistance	RON32P	-	230	370	mΩ	Vo3=5.0V, ILx32=-50mA
Lx32 Lowside SW on resistance	RON32N	-	115	185	mΩ	ILx32=+50mA
Lx4 Highside SW on resistance	RON4P	-	170	290	mΩ	ILx4=-50mA
Lx4 Lowside SW on resistance	RON4N	-	140	230	mΩ	ILx4=+50mA
Lx1,Lx2,Lx4 terminal discharge resistance	RDISLX,2,4	40	100	160	Ω	CTL1,2,4=0V
VO3 terminal discharge resistance	RDISVO3	40	100	160	Ω	CTL3=0V
【Power Good】						
PG terminal on resistance	RONPG	-	350	600	Ω	PG=1V
PG terminal leak current	ILKPG	-	0	1.0	μA	PG=15V
CH1G,CH2G terminals high voltage	CH1,2GH	VREGA -0.5	-	-	V	ICTL1,2G=-100uA
CH1G,CH2G terminals low voltage	CH1,2GL	-	-	0.5	V	ICTL1,2G=+100uA
【Control】						
CTL terminal active voltage	VCTLH	2.5	-	VCC	V	CTL1,2,3,4
CTL terminal stand-by voltage	VCTLL	-0.3	-	0.8	V	CTL1,2,3,4
CTL terminal pull-down resistance	RCTL	250	400	700	kΩ	CTL1,2,3,4
SEL terminal high voltage	VSELH	2.5	-	VCC	V	
SEL terminal low voltage	VSELL	-0.3	-	0.8	V	
SEL terminal pull-down resistance	RSEL	250	400	700	kΩ	
【Circuit Current】						
Stand-by current(IC OFF)	ISTB	-	0	5	μA	CTL1-4=0V
Active current(SCP detect state)	ICCST	-	5	10	mA	INV1,2,3,4=0V Circuit current of analog
Active current(DC/DC converter active)	ICCAPP	-	35	45	mA	All channels operate with recommended external parts

●**Application circuit1**

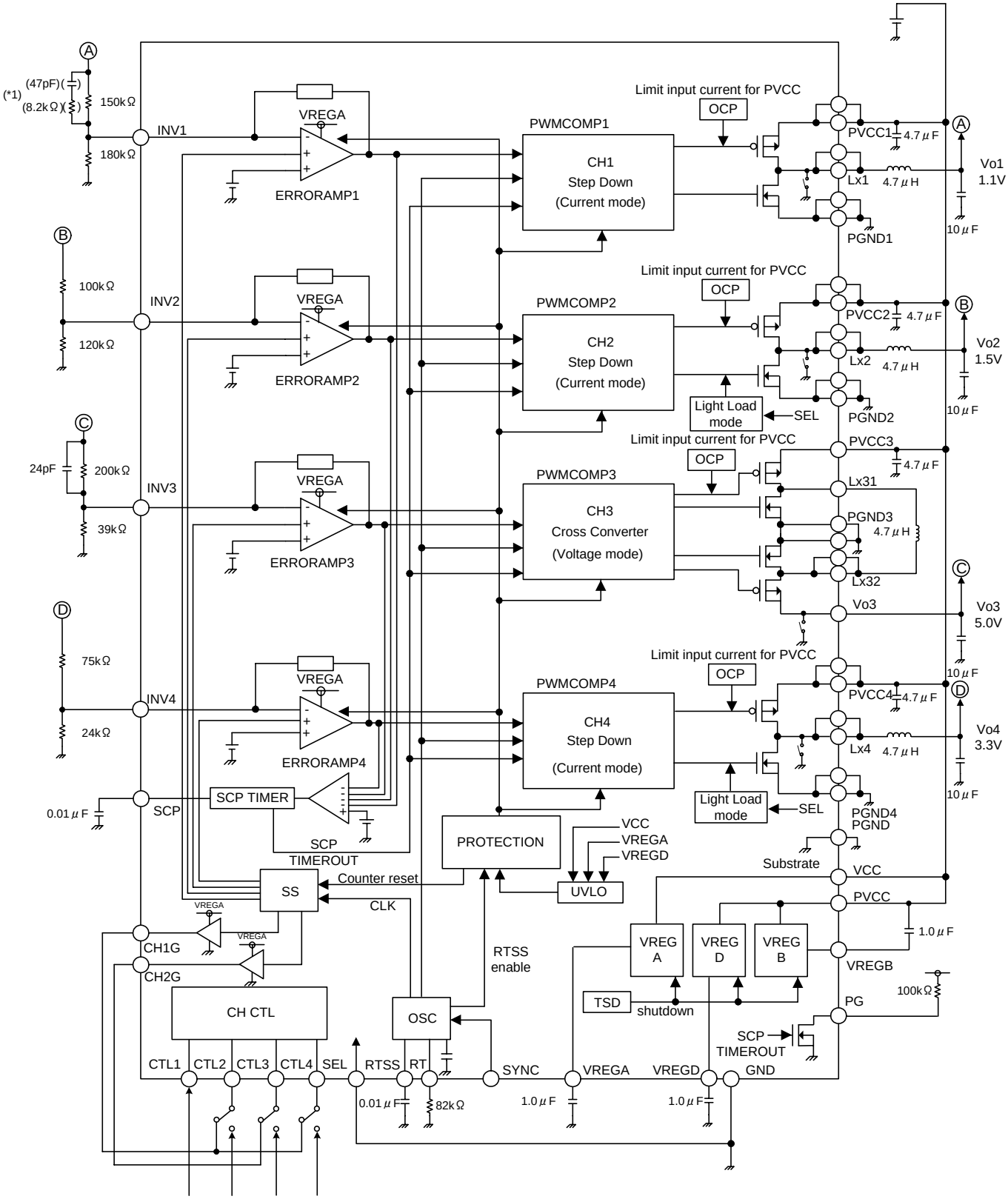

Figure. 4 Application circuit 1

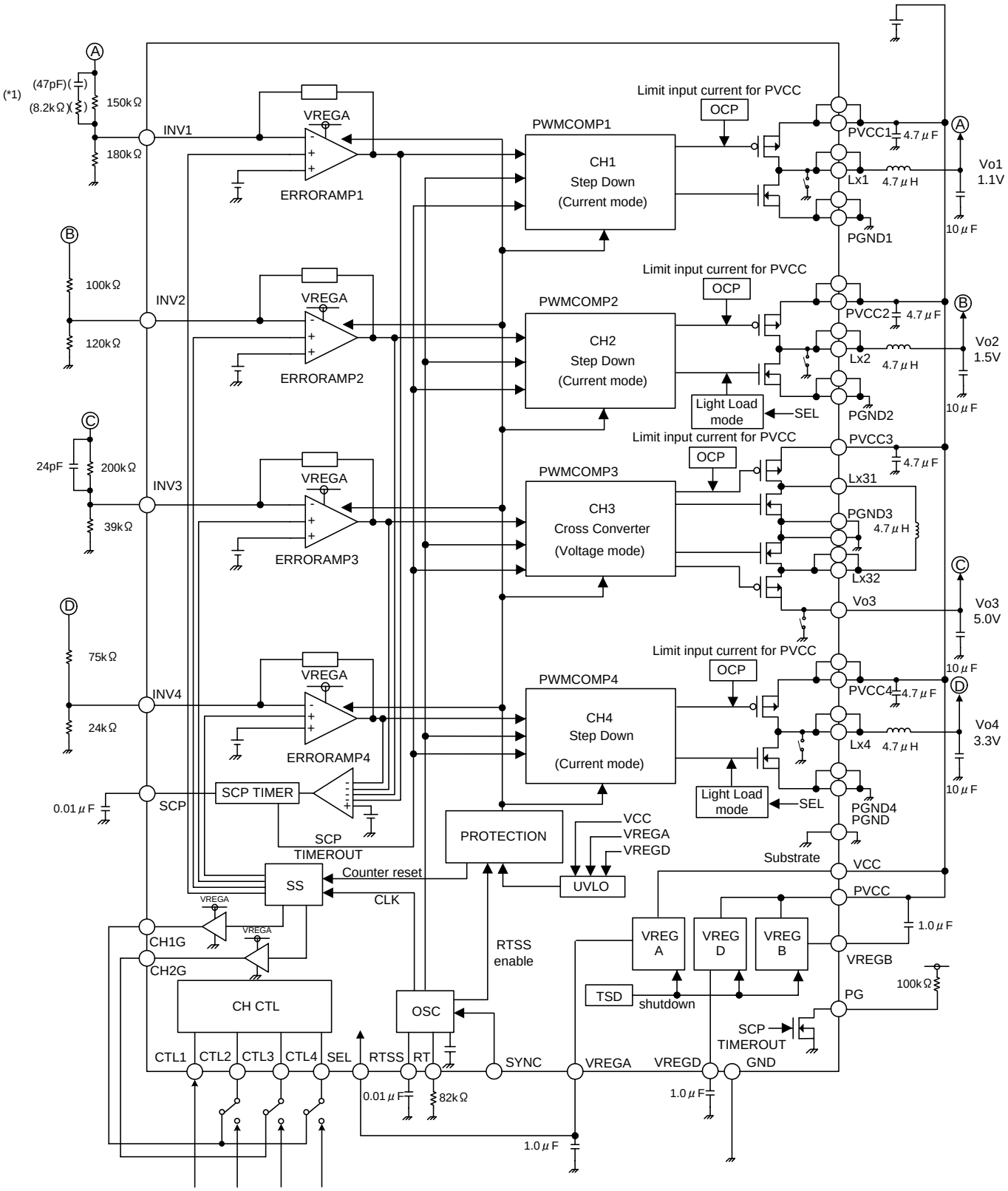

Figure. 5 Application circuit 2

(*1) Add to improve transient characteristics optionally.
We are confident that above applied circuit diagram should be recommended, but please thoroughly confirm its characteristics when using it. In addition, when using it with external circuit's constants changed, please make a decision that allows a sufficient margin in light of the fluctuations of external components and ROHM's IC in terms of not only static characteristics but also transient characteristics..

●**Timing Chart of startup**

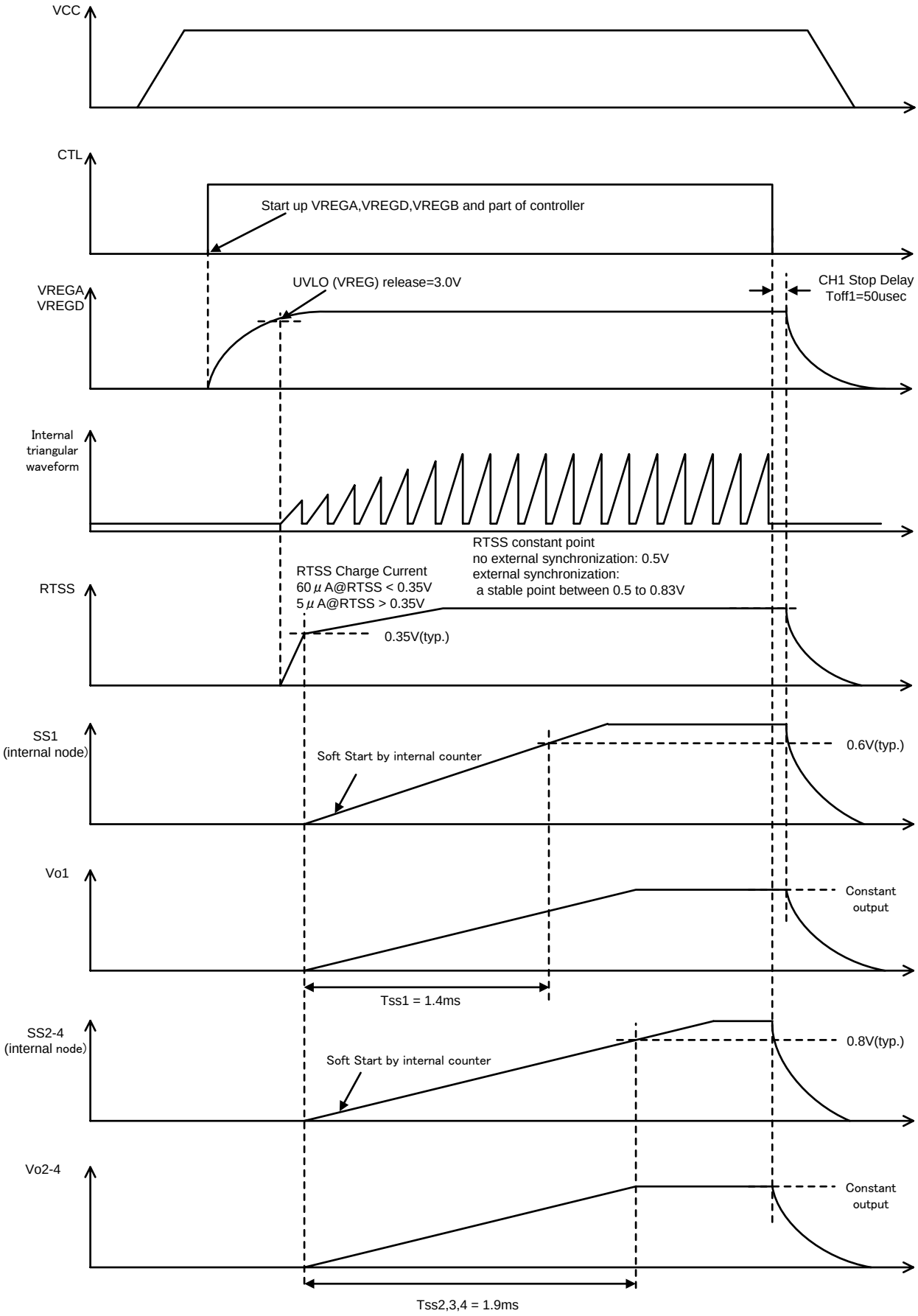

Figure.6 Timing chart of Startup

●**Timing chart of UVLO operation**

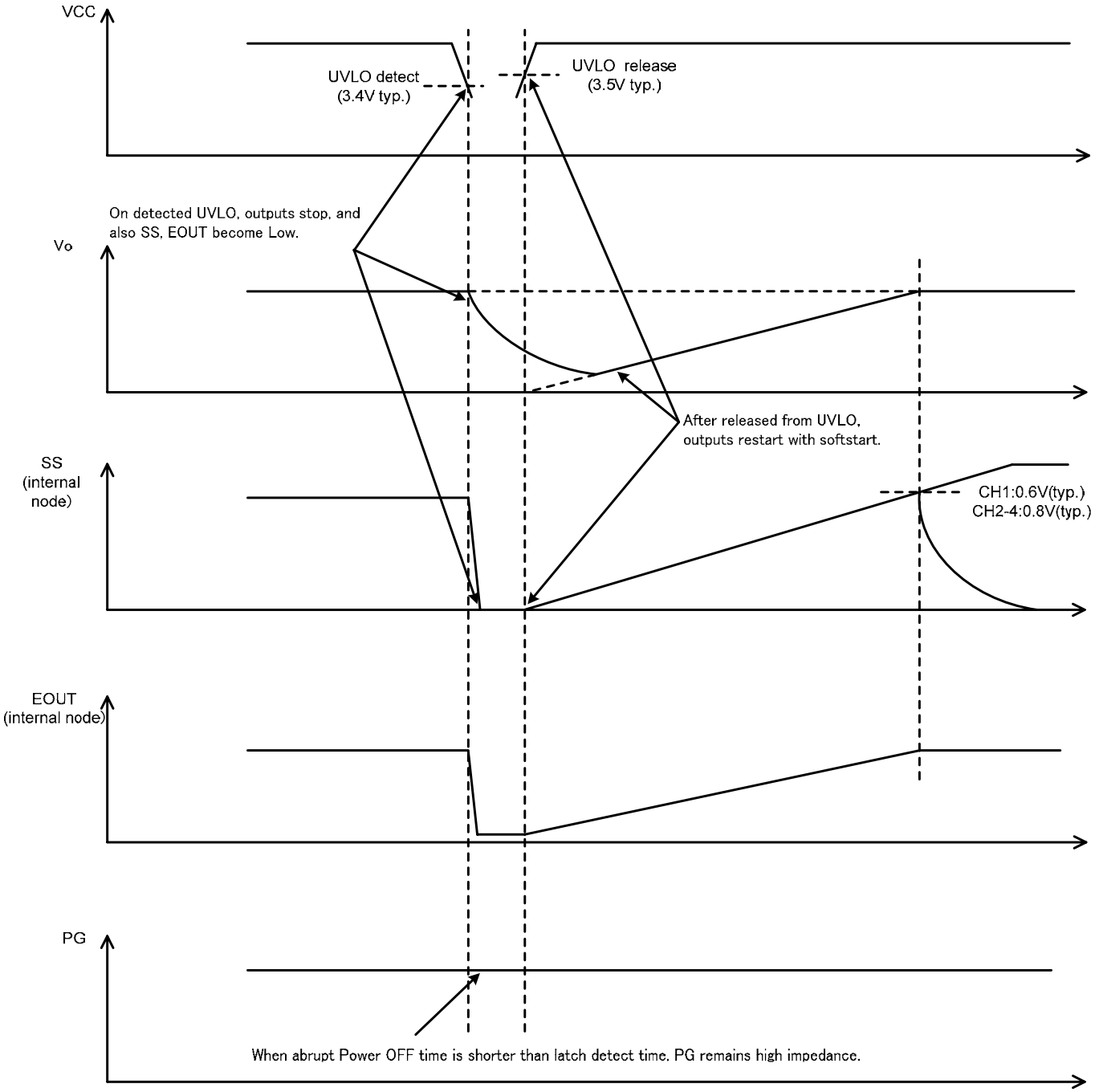

Figure. 7 Timing chart of UVLO operation
(UVLO detect and after release from UVLO, restart with softstart)

●**Timing chart of SCP detection after startup**

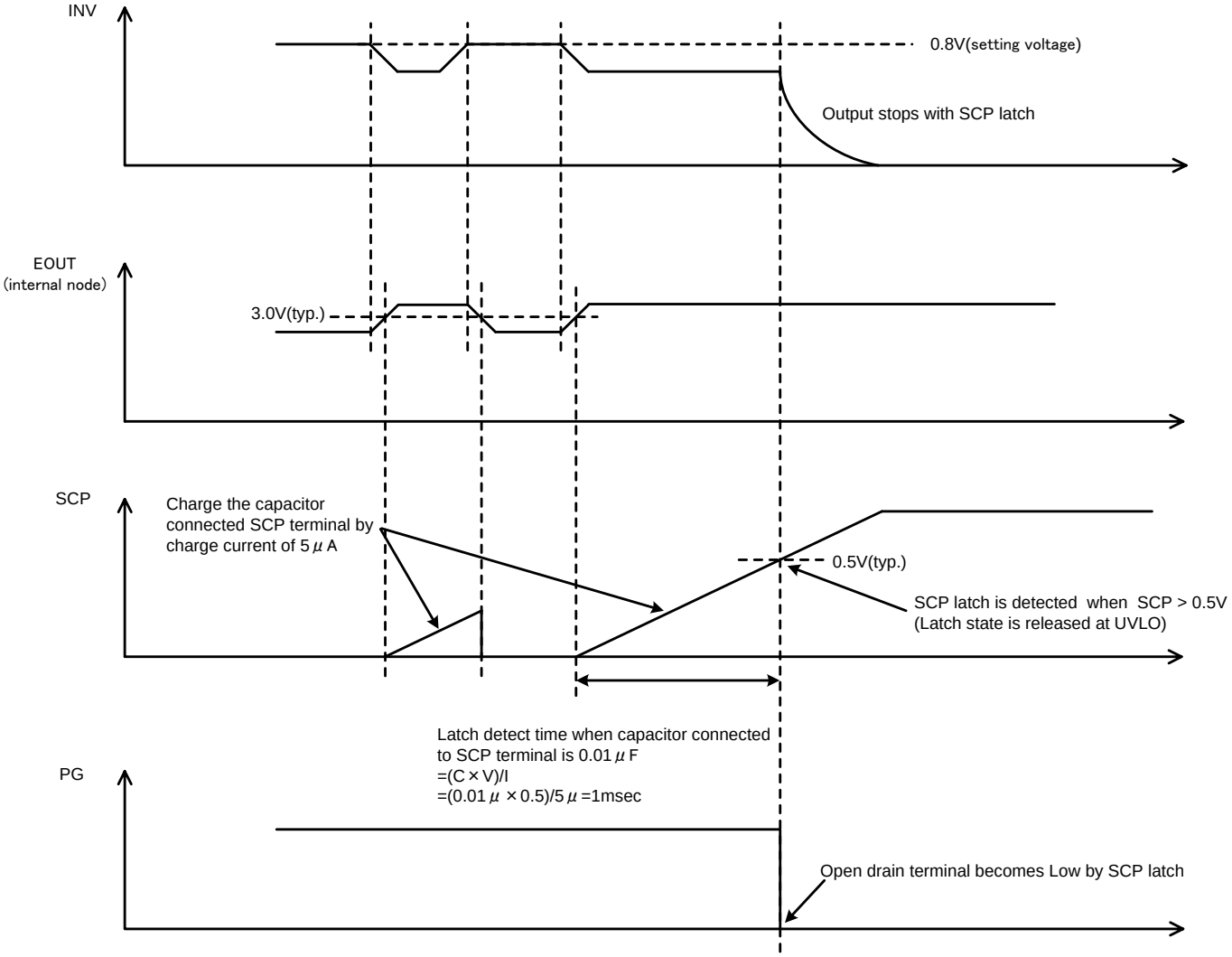

Figure. 8 Timing chart of SCP detection after startup
(abnormal output in operating)

●**Timing chart of startup with output shorted to GND**

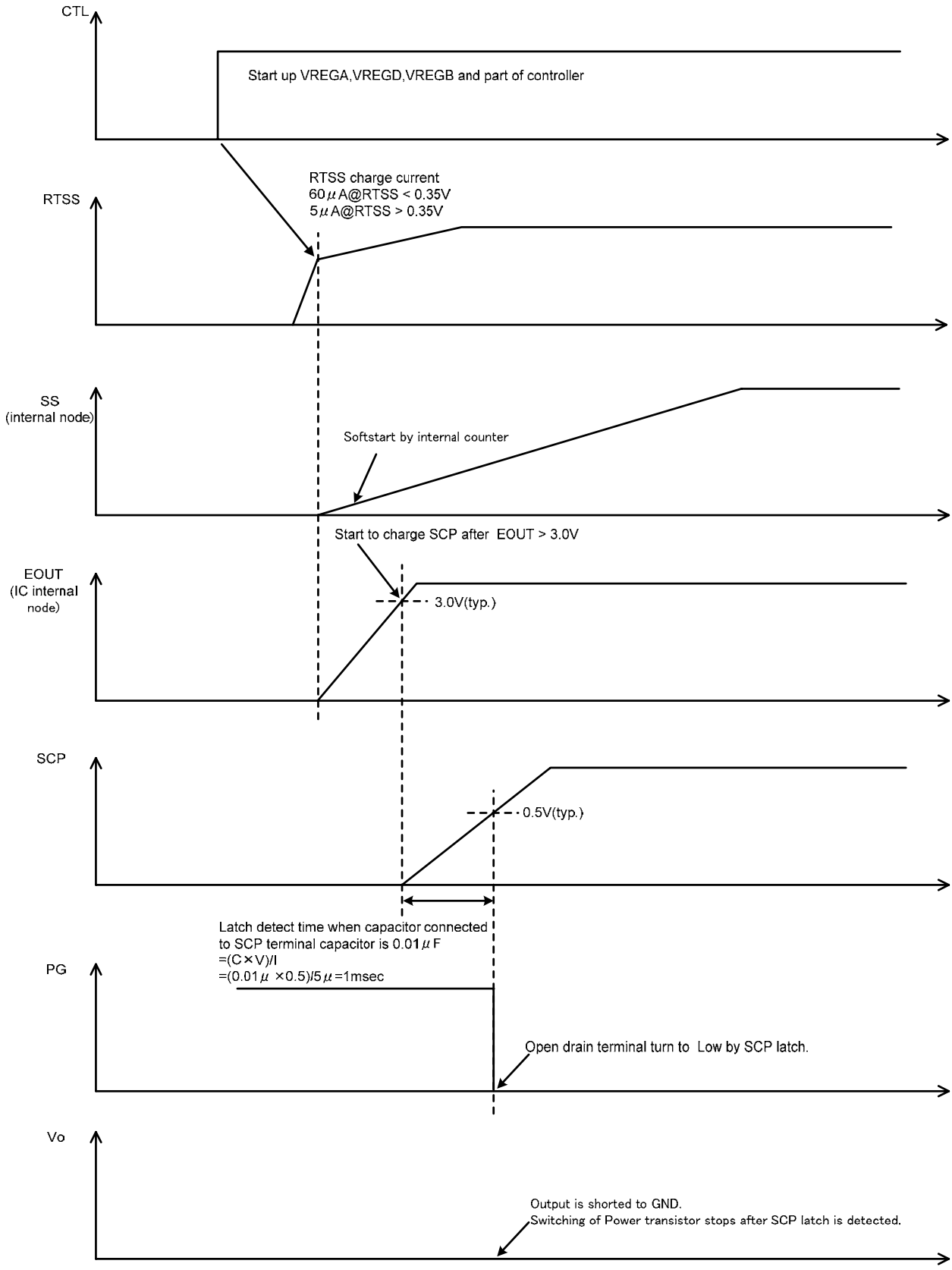

Figure. 9 Timing chart of startup with output shorted to GND

●**Typical Operating Characteristics**

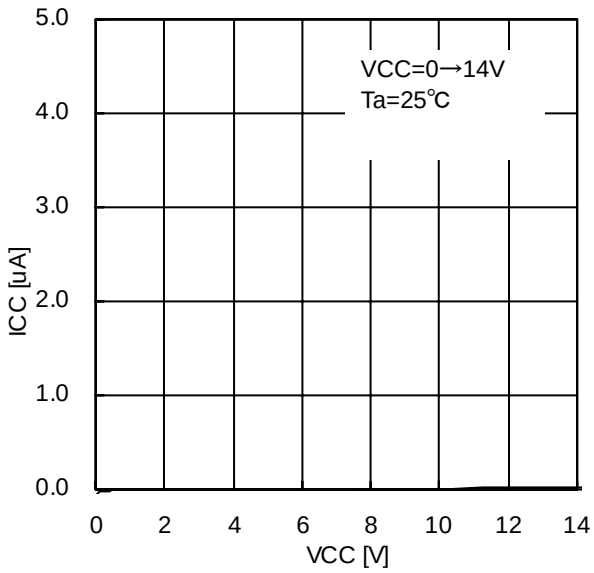

Figure.10 ICC(OFF) - VCC

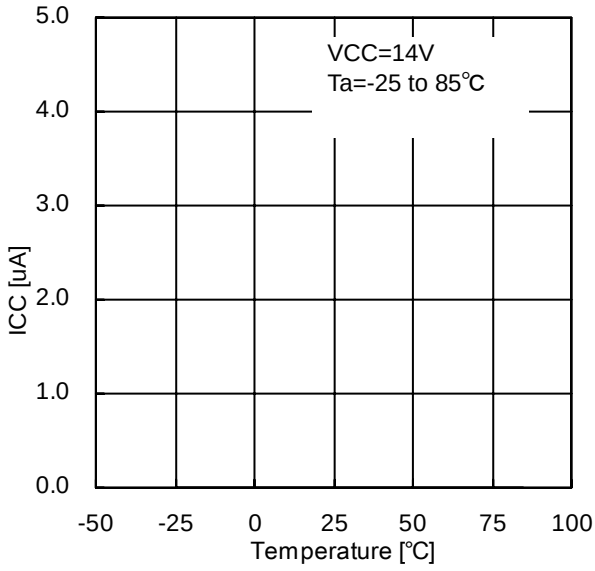

Figure.11 ICC(OFF) - Ta

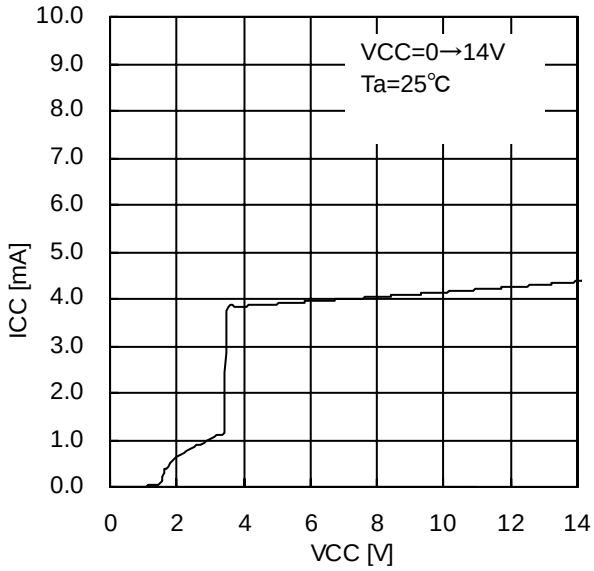

Figure.12 ICC(SCP state) - VCC

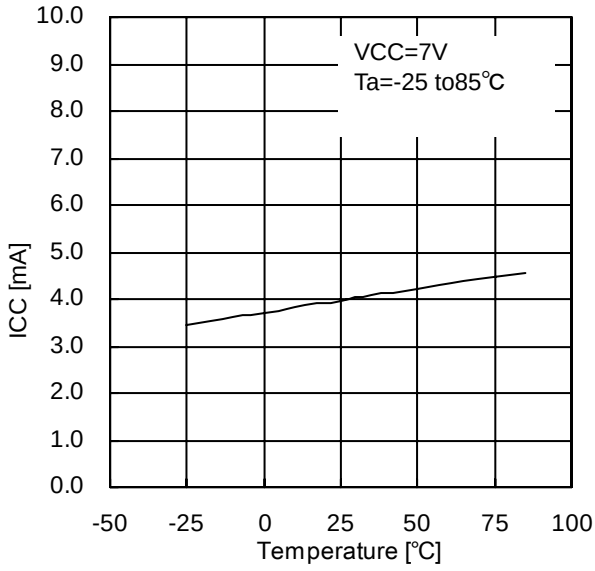

Figure.13 ICC(SCP state) - Ta

●**Typical Operating Characteristics(continued)**

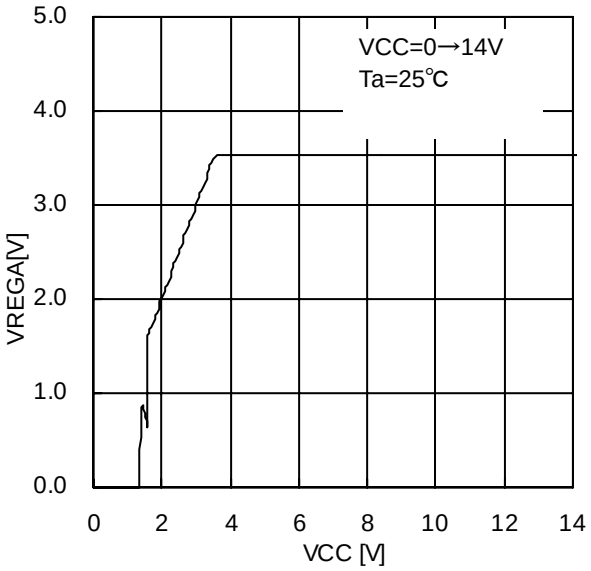

Figure.14 VREGA - VCC

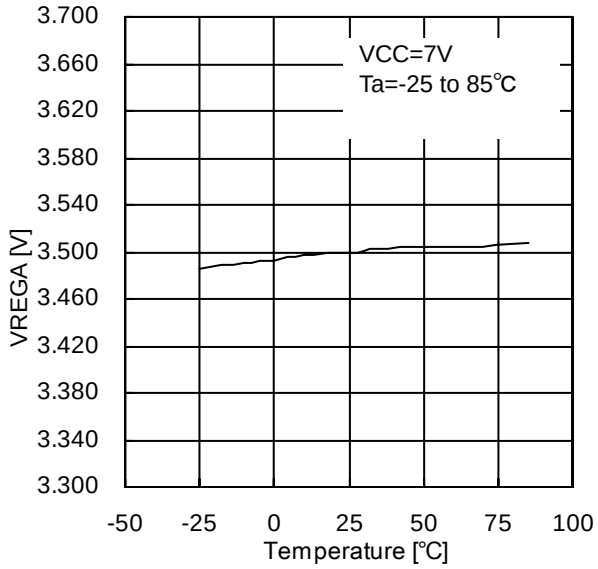

Figure.15 VREGA – Ta

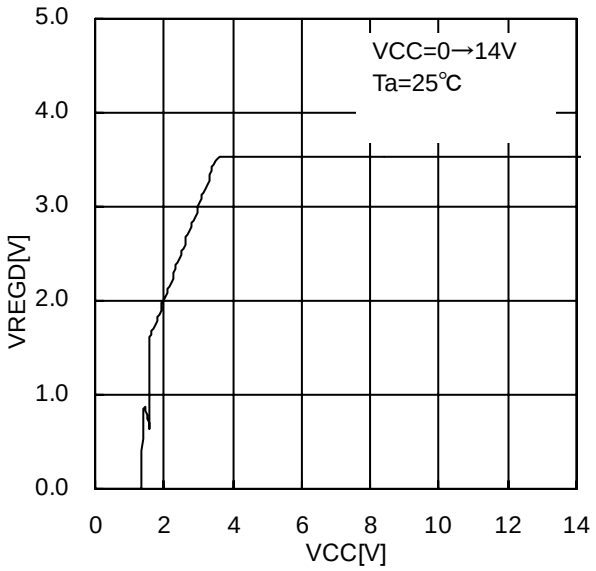

Figure.16 VREGD- VCC

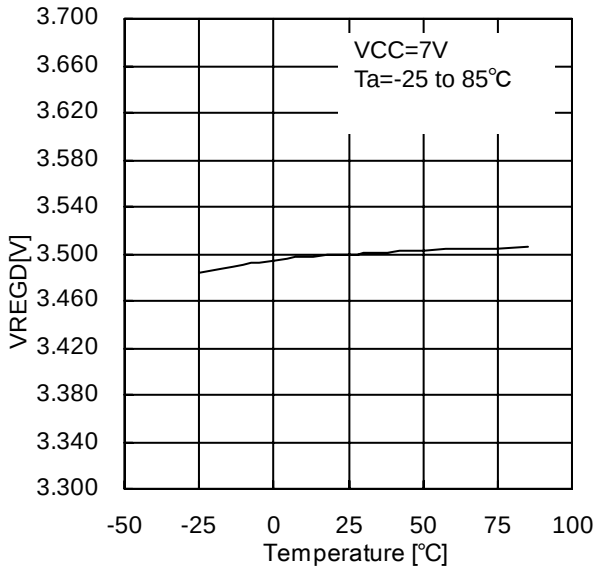

Figure.17 VREGD – Ta

●**Typical Operating Characteristics(continued)**

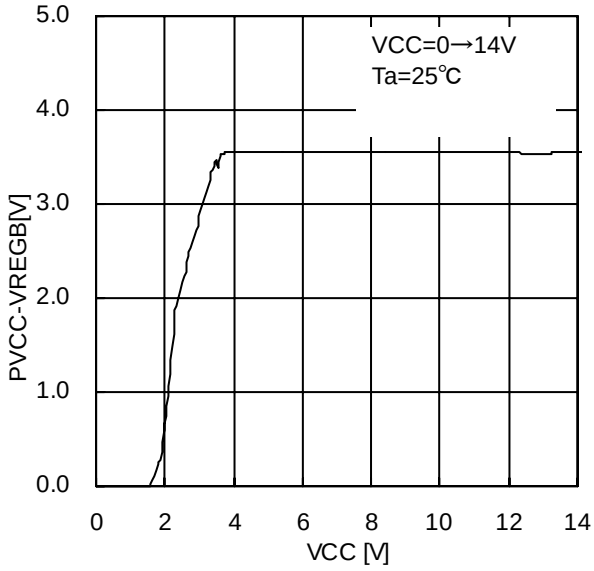

Figure.18 (PVCC–VREGB)- VCC

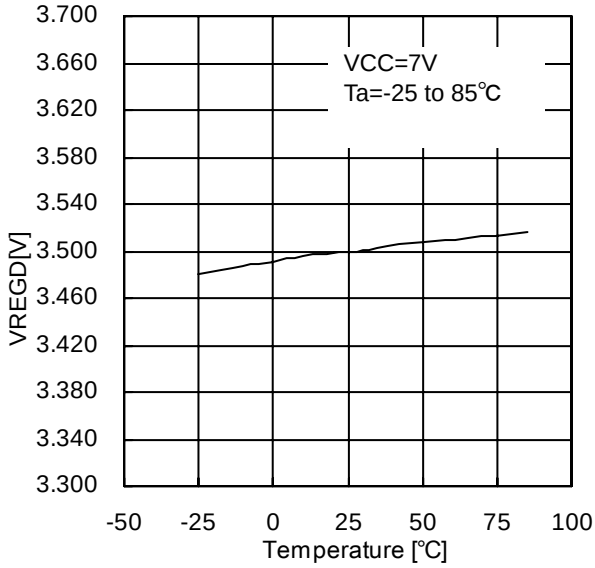

Figure.19 (PVCC–VREGB) – Ta

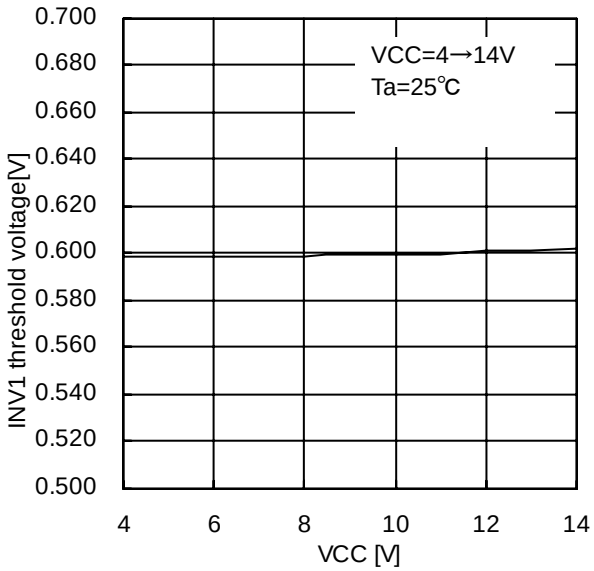

Figure.20
INV1 threshold voltage – VCC

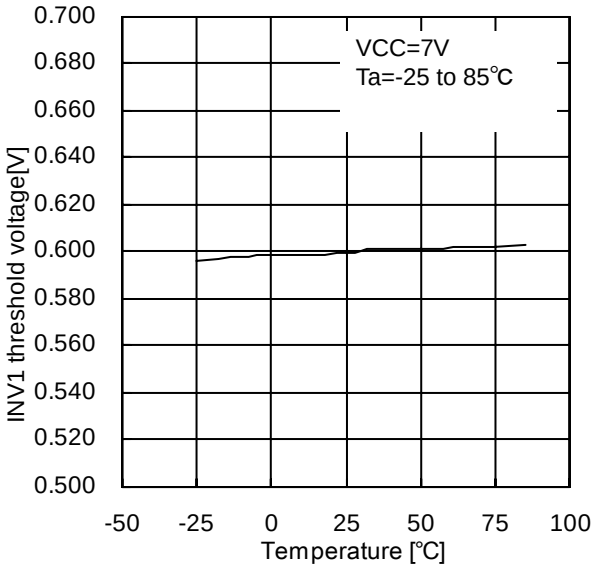

Figure.21
INV1 threshold voltage – Ta

●**Typical Operating Characteristics(continued)**

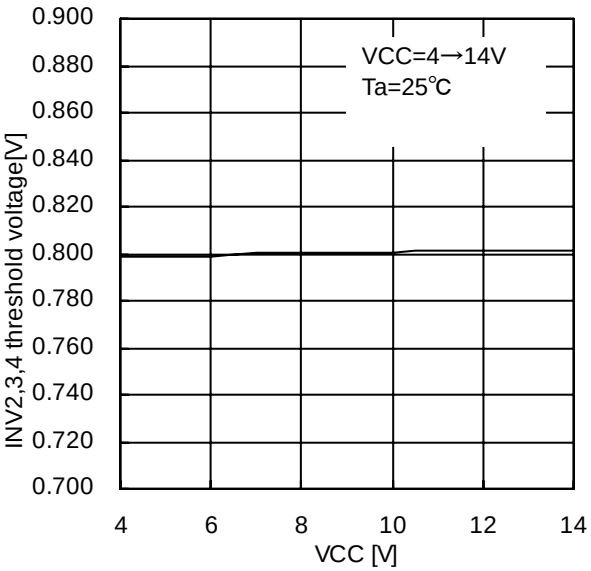

Figure.22
INV2,3,4 threshold voltage– VCC

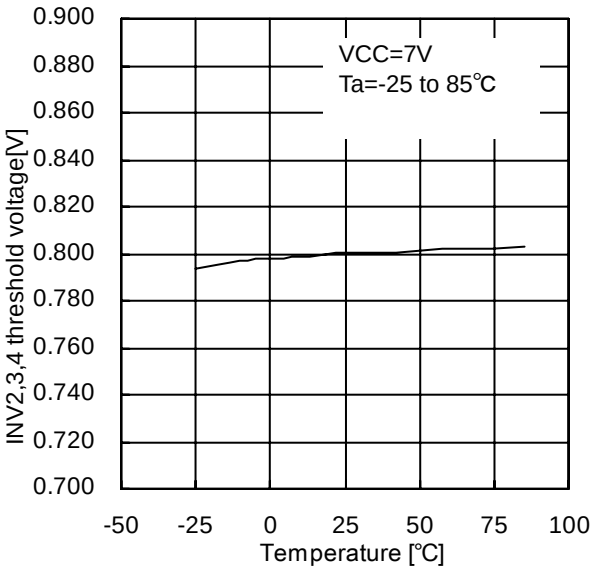

Figure.23
INV2,3,4 threshold voltage– Ta

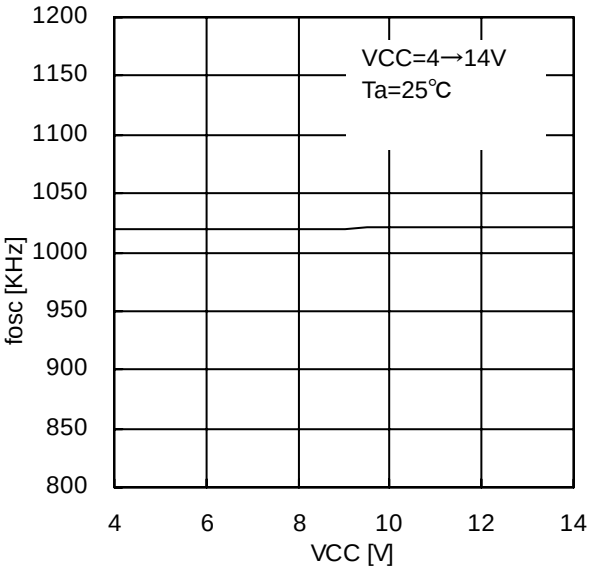

Figure.24 fosc - VCC

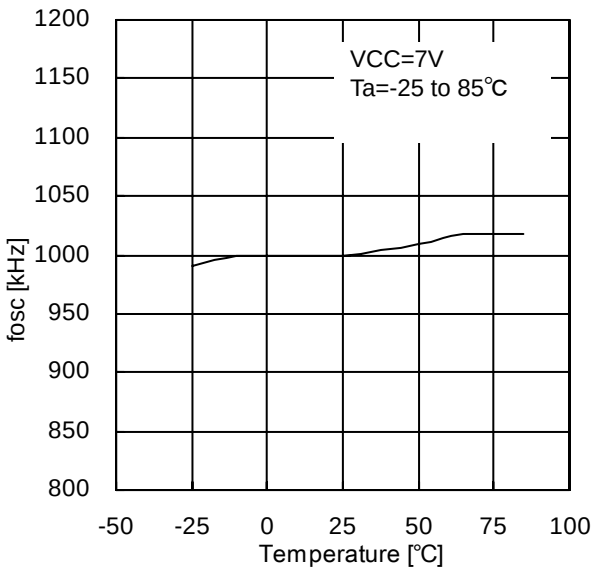

Figure.25 fosc - Ta

●**Typical Operating Characteristics(continued)**

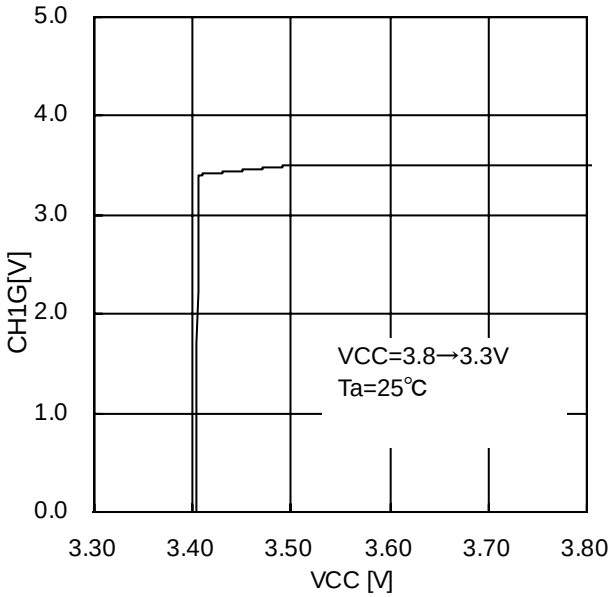

Figure.26 UVLO VCC
detect threshold voltage

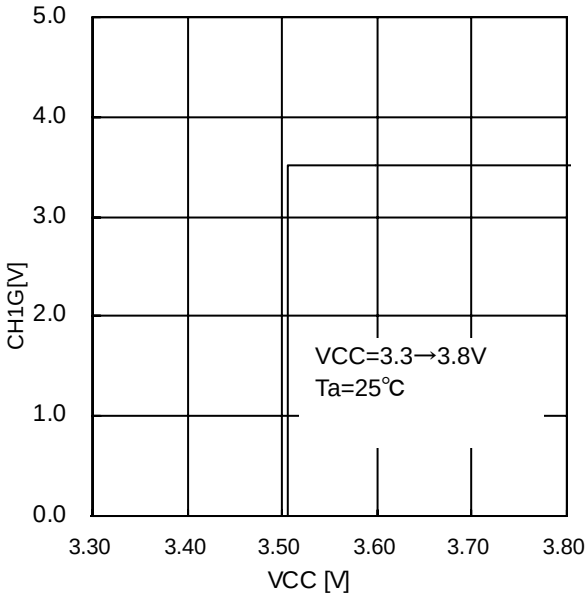

Figure.27 UVLO VCC
reset threshold voltage

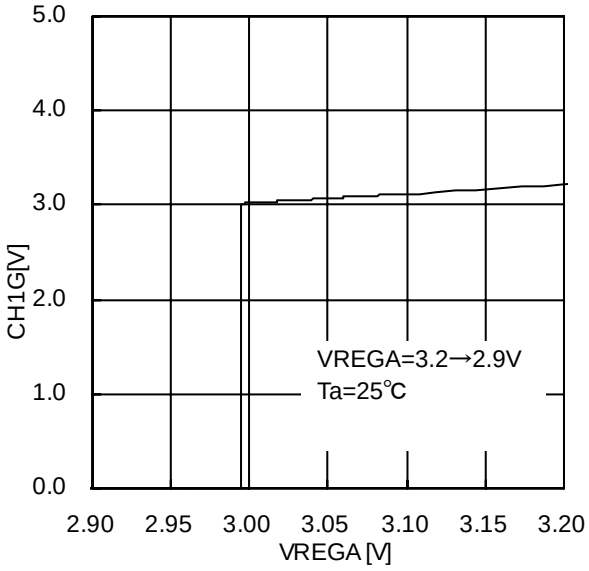

Figure.28 UVLO VREGA
detect threshold voltage

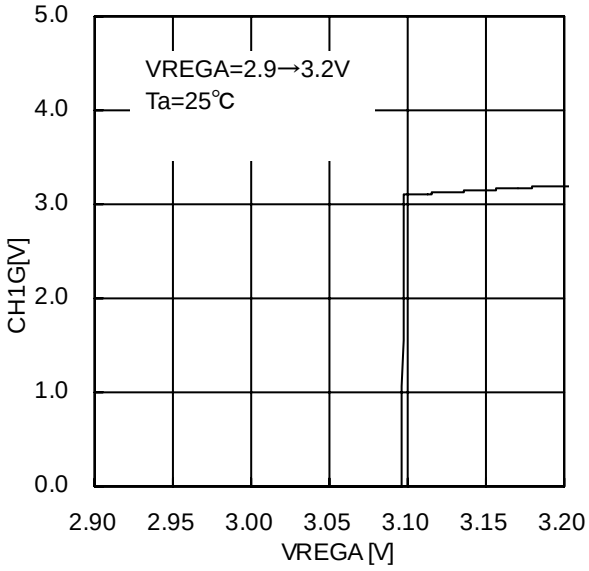

Figure.29 UVLO VREGA
reset threshold voltage

●**Typical Operating Characteristics(continued)**

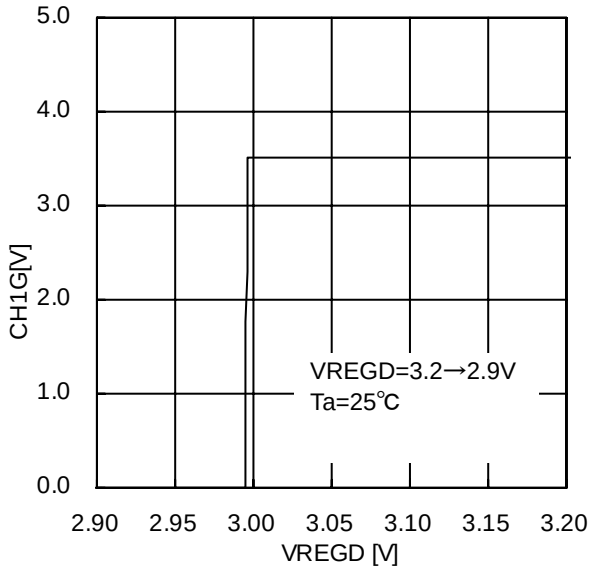

Figure.30 UVLO VREGD detect threshold voltage

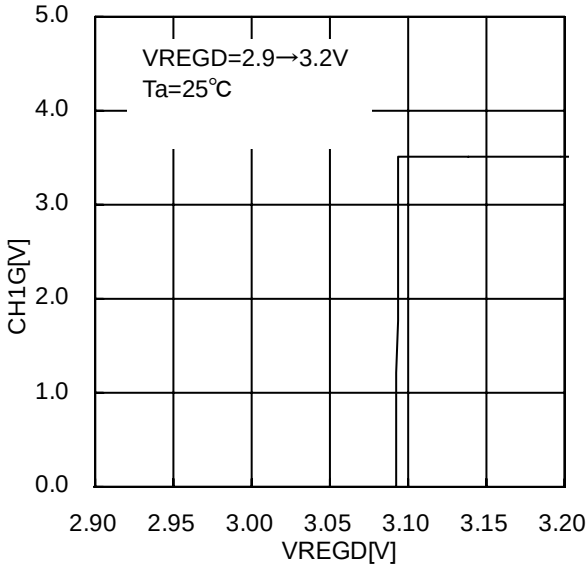

Figure.31 UVLO VREGD reset threshold voltage

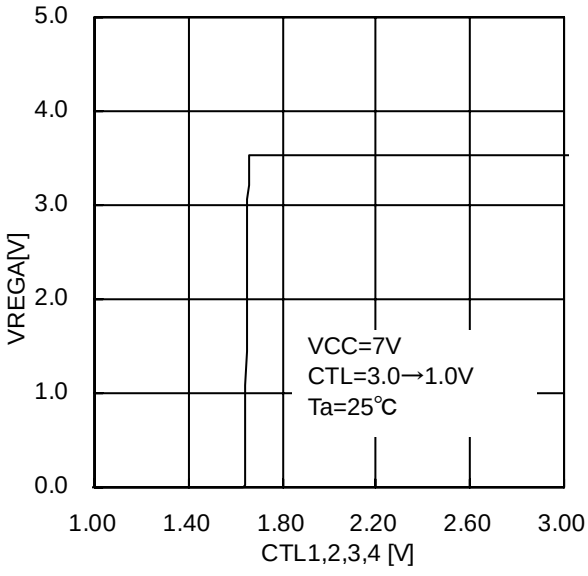

Figure.32 CTL OFF threshold voltage

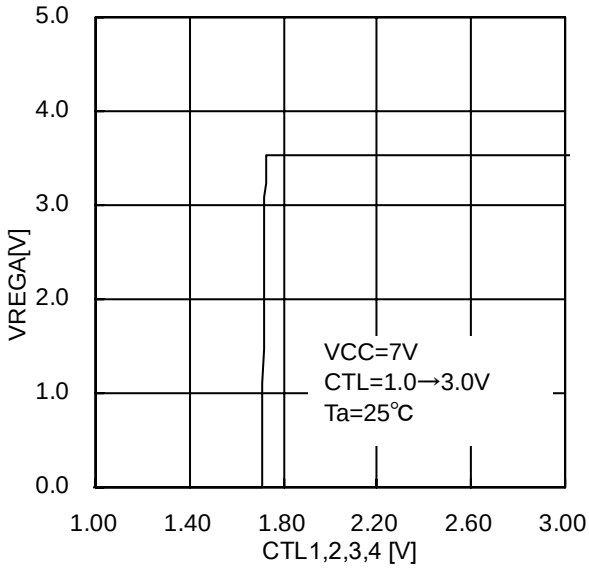

Figure.33 CTL ON threshold voltage

●**Typical Operating Characteristics(continued)**

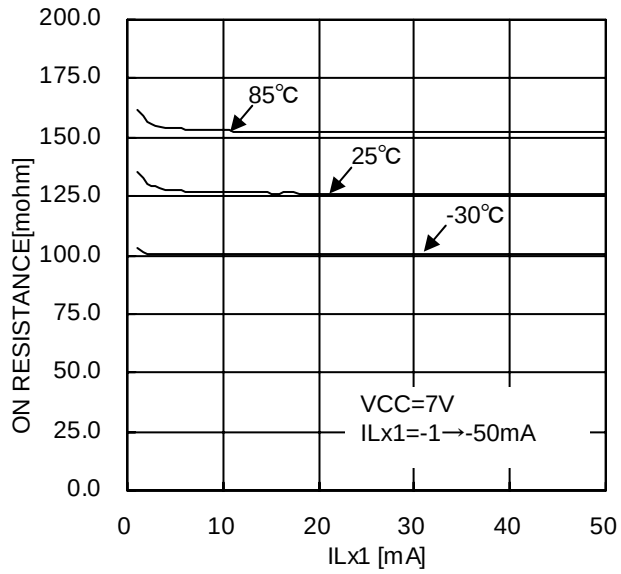

Figure.34 Lx1 High side FET RON
(Ta=-30℃, 25℃, 85℃)

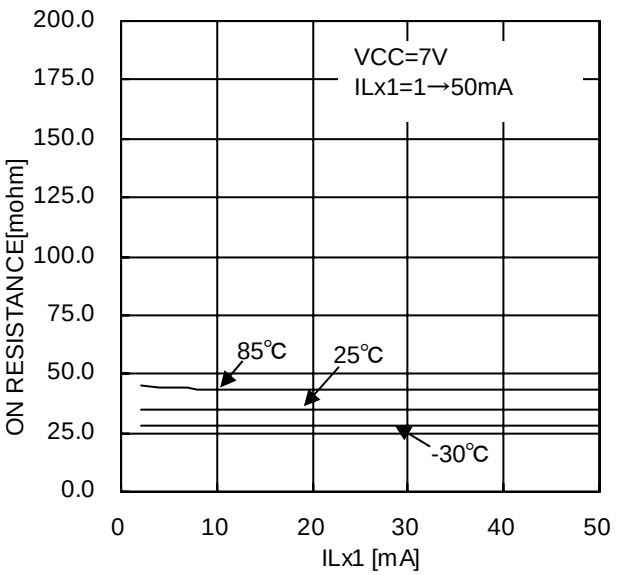

Figure.35 Lx1 Low side FET RON
(Ta=-30℃, 25℃, 85℃)

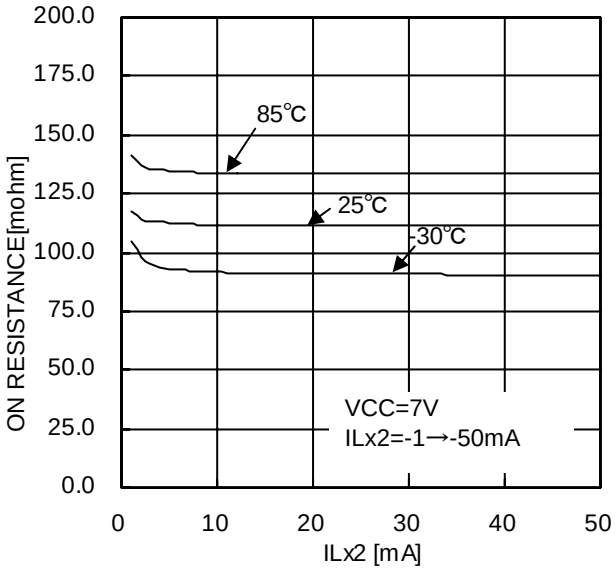

Figure.36 Lx2 High side FET RON
(Ta=-30℃, 25℃, 85℃)

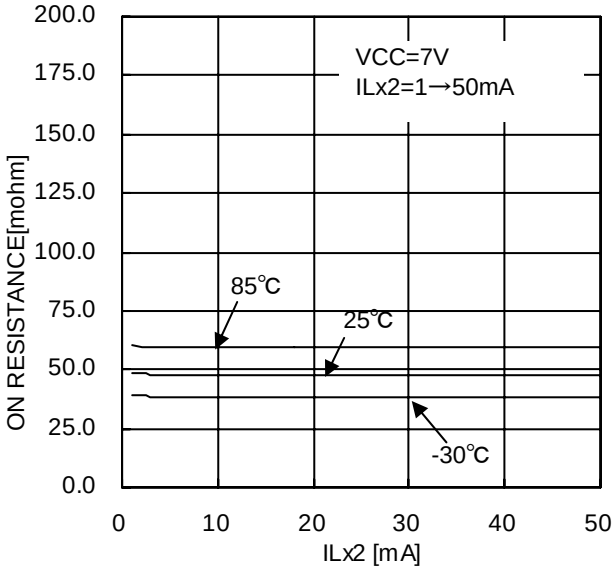

Figure.37 Lx2 Low side FET RON
(Ta=-30℃, 25℃, 85℃)

●**Typical Operating Characteristics(continued)**

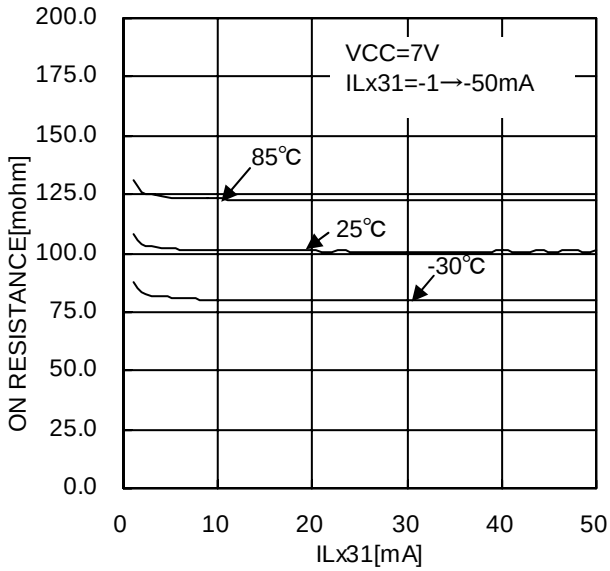

Figure.38 Lx31 High side FET RON
(Ta=-30℃, 25℃, 85℃)

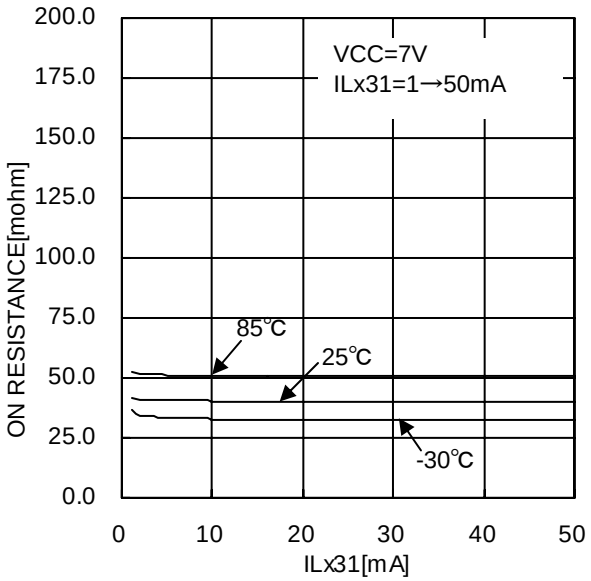

Figure.39 Lx31 Low side FET RON
(Ta=-30℃, 25℃, 85℃)

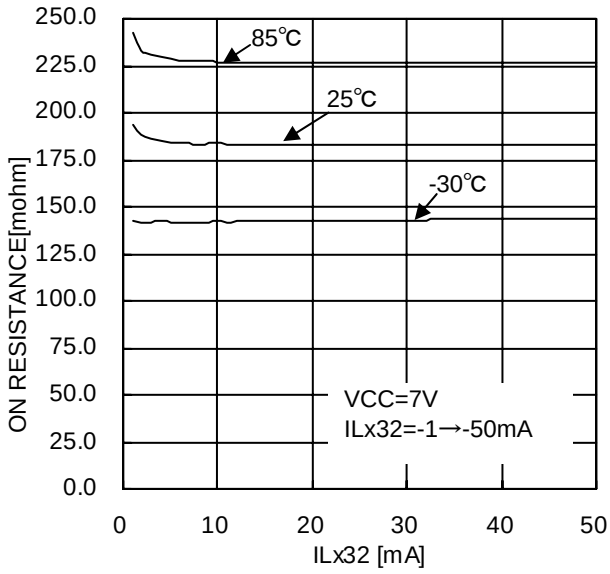

Figure.40 Lx32 High side FET RON
(Ta=-30℃, 25℃, 85℃)

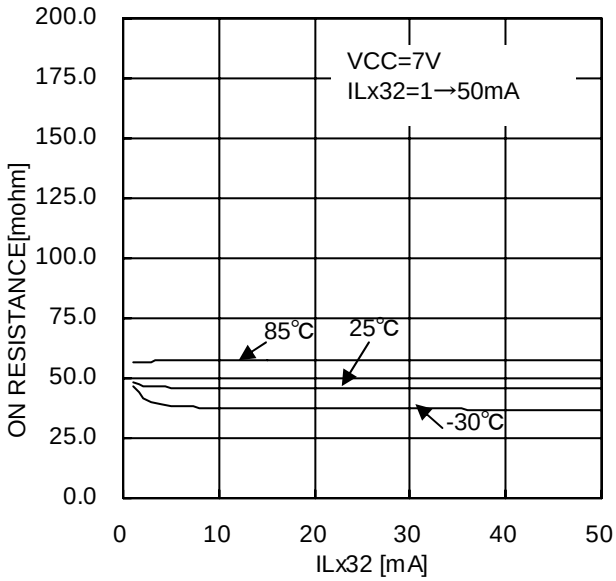

Figure.41 Lx32 Low side FET RON
(Ta=-30℃, 25℃, 85℃)

●**Typical Operating Characteristics(continued)**

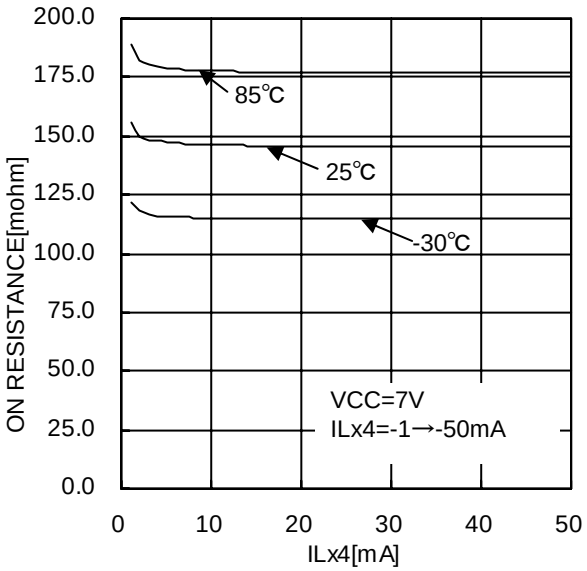

Figure.42 Lx4 High side FET RON
(Ta=-30℃, 25℃, 85℃)

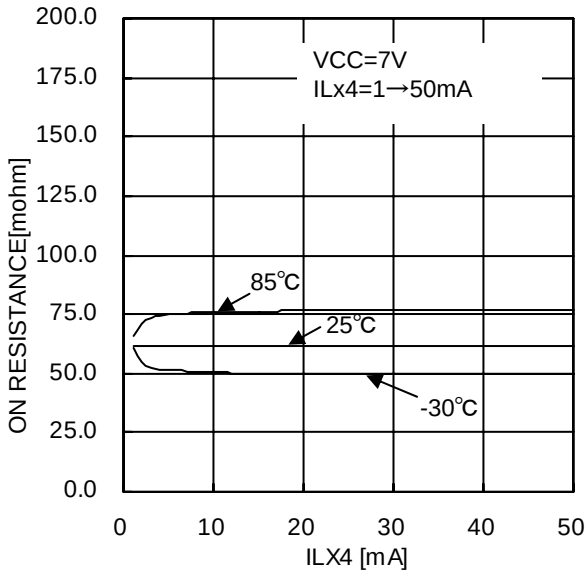

Figure.43 Lx4 Low side FET RON
(Ta=-30℃, 25℃, 85℃)

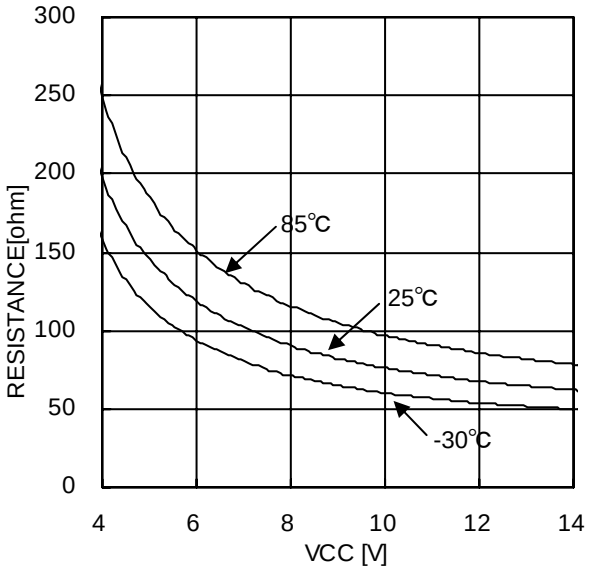

Figure.44 Lx1 discharge SW RON
(Ta=-30℃, 25℃, 85℃)

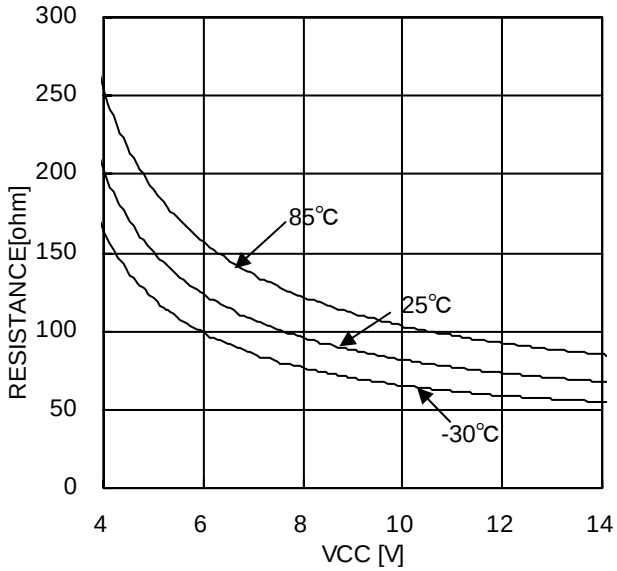

Figure.45 Lx2 discharge SW RON
(Ta=-30℃, 25℃, 85℃)

●**Typical Operating Characteristics(continued)**

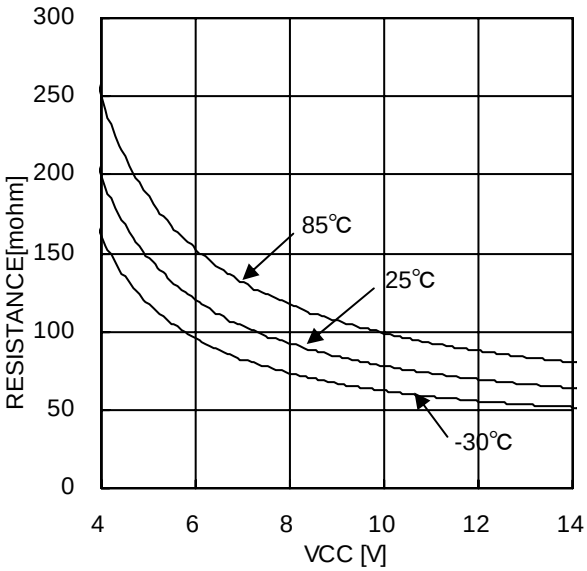

Figure.46 Vo3 discharge SW RON
(Ta=-30℃, 25℃, 85℃)

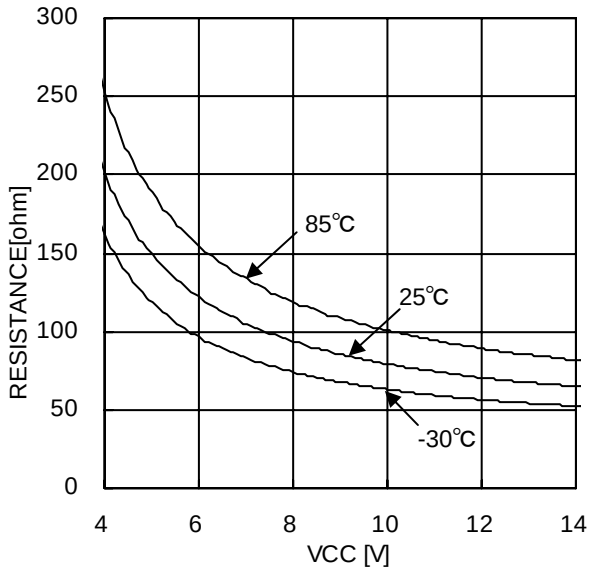

Figure.47 Lx4 discharge SW RON
(Ta=-30℃, 25℃, 85℃)

●**Efficiency**

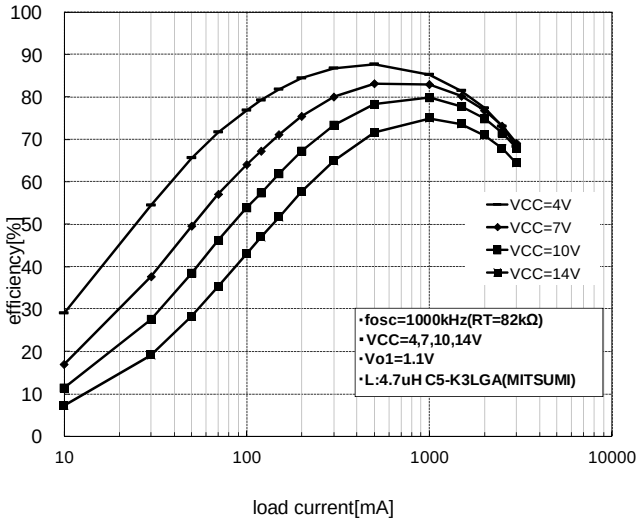

Figure.48 Efficiency – load current
CH1 Vo1=1.1V

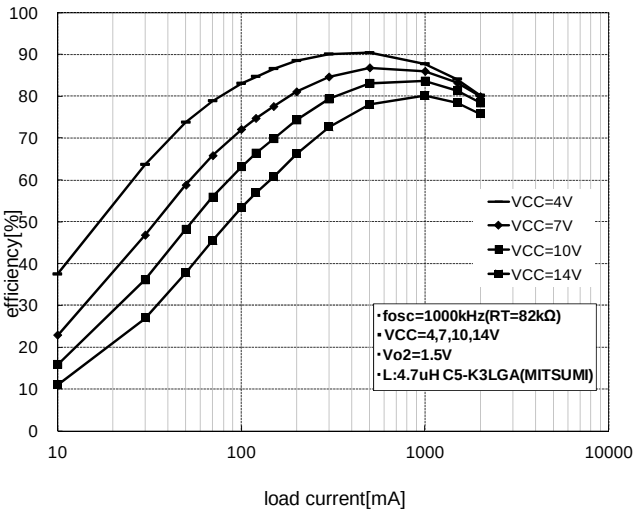

Figure.49 Efficiency – load current
CH2 Vo2=1.5V

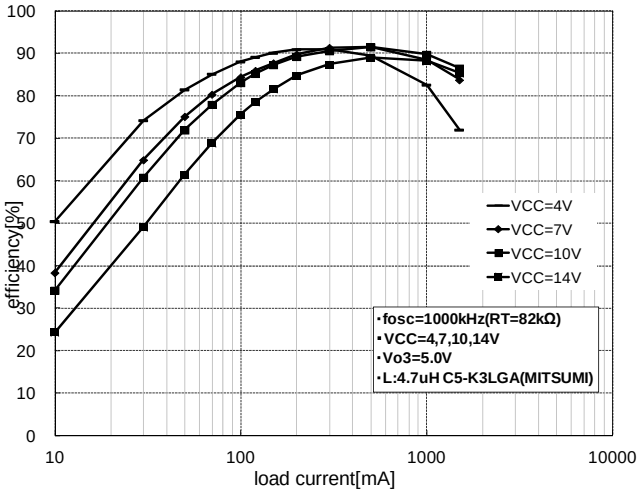

Figure.50 Efficiency – load current
CH3 Vo3=5.0V

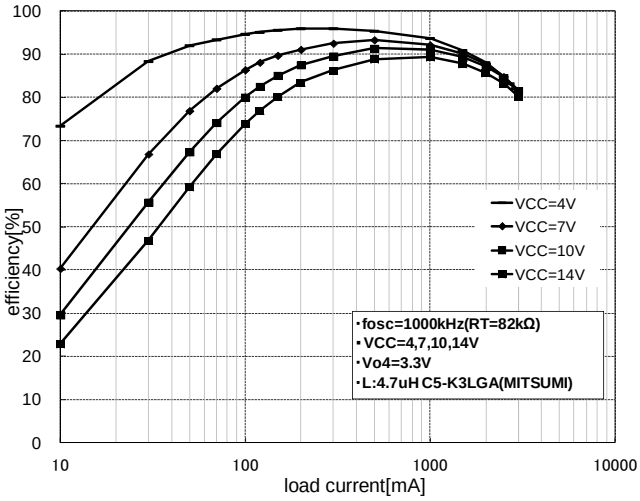

Figure.51 Efficiency – load current
CH4 Vo4=3.3V

●Block explanation

・DCDC Block(4channels)

Followings is specification of each channel of this IC.

	CH1	CH2	CH3	CH4
Type	Buck	Buck	Buck-Boost	Buck
Mode	Current	Current	Voltage	Current
Synchronous rectifier	○	○	○	○
FET constitution	Internal P/N	Internal P/N	Internal P/N	Internal P/N
Softstart	Internal counter	Internal counter	Internal counter	Internal counter
ON/OFF control	Independent	Independent	Independent	Independent

Table.1 specification of each channel

・VREGA,VREGD,VREGB Block

VREGA is an internal regulator of 3.5V output. VREGD supply 3.5V gate bias voltage of Low side internal FET, VREGB supply PVCC − 3.5V gate bias voltage of High side internal FET. Bypass these regulators to GND(VREGB to PVCC) with a capacitor between 0.47μF and 2.2μF. We recommend capacitor of 1.0μF.

・Oscillator Block

OSC generates triangular waveform (slope waveform) with a resistor connected to RT terminal for setting frequency and inputs into PWM comparator of each CH. Swithing frequency is set to 1.0MHz at RT = 82kΩ. Refer to the way of detailed setting on p.26.

When CTL is turned ON with SYNC terminal input external clock, DC/DC converter switches at the frequency of the clock input to SYNC terminal. Refer to p.29 for details of external synchronization.

・ERRORAMP Block

Error amplifiers monitor output voltage at INV terminals and output amplified error voltage at internal EOUT node. Reference voltage of CH1 is 0.6V and accuracy is ±1.67%, and 0.8V for CH2-4 and accuracy is ±1.25%. Refer to p.26 for setting of output voltage.

・PWM Comparator Block

PWM comparators control switching duty of output FET by comparing SLOPE waveform from OSC and output voltage of error amplifier.

・Current Mode Control Block

CH1, 2 and 4 operate with current mode PWM. In current mode DC/DC converter, main FET of synchronous rectifier turns on at the edge of main clock, and turn off after detection of peak current in current comparator.

・Buck-Boost control Block

a block for controlling the switching duty of buck-boost DC/DC of CH3. This block consists of PWM comparator to compare 1.0MHz SLOPE waveform and output of error amplifier, and Logic circuit to convert the output of PWM comparator to ON/OFF signal of 4 internal output FETs.

・Softstart Block(SS)

Softstart block prevents the inrush current to charge the output capacitor at DC/DC start-up by softly starting up the reference voltage of error amplifier. CH1 is 1.4msec(typ. at fosc=1MHz) and CH2-4 are 1.9msec(typ. at fosc=1MHz.)

Only CH1 has 50usec of delay time at stop. As in Figure .6, output is turned off after 50usec has passed from CTL1 is turned to L.

・Channel Control Block(CH_CTL)

CTL1-4 terminals enable output of each channels to turn ON/OFF individually. When voltage of each terminal is over 2.5V and less than VCC voltage each channel turns ON, and when the terminals are open or voltage of them is over -0.3V and less than 0.8V, it turns OFF. When all channels are turned OFF, IC becomes stand-by state. Each terminal contains pull-down resistor of 400kΩ (typ.) Note that the output voltage of CH3 may swing when CH4 is turned OFF while CH3 is operating, so use this IC after confirming with much care that does not cause any problems in that situation.

CTL				LX					VREGA	VREGD	VREGB	OSC
1	2	3	4	1	2	31	32	4				
L	L	L	L	L	L	Z	L	L	N	N	N	N
H	L	L	L	A	L	Z	L	L	A	A	A	A
L	H	L	L	L	A	Z	L	L	A	A	A	A
L	L	H	L	L	L	A	A	L	A	A	A	A
L	L	L	H	L	L	Z	L	A	A	A	A	A
H	H	H	H	A	A	A	A	A	A	A	A	A

Table.2 CTL table

・Short Circuit Protection Circuit(SCP)

Output short protect circuit with timer latch. When output of any channels drop, output of error amplifier rises. And after it reaches to 3.0V (typ.), SCP block start to charge the output capacitor at SCP terminal with current of 5uA output of all channels stop when the terminal voltage of SCP reaches to 0.5V. To release short circuit protection latch state, turn CTL terminal to “L” level and return to “H”, or restart power supply. When you don’t use short circuit protection, connect SCP terminal to GND. Refer to p.11, 12 about timing chart of SCP operation.

・Undervoltage Lock Out(UVLO)

Undervoltage lock out prevents IC malfunctions that could otherwise occur due to power supply fluctuation at power on or abrupt power off. This system turns off output of each channel and fix the output voltage of error amplifier to “L” when the VCC voltage becomes lower than 3.4V(typ.), or anyone of VREGA, VREGD voltage becomes lower than 3.0V(typ.) Threshold voltage of each UVLO has hysteresis of 0.1V to prevent malfunctions in transient swing of power supply around threshold voltage. Refer to p.10 about timing chart of UVLO operation.

・Thermal Shut Down(TSD)

The thermal shutdown circuit is protection the IC against thermal runaway and heat damage. When the temperature reaches to TSD threshold (typ. 175℃), the output of all channels, VREGA, VREGD, VREGB are turned off. Threshold of TSD has hysteresis of 25℃ to prevent malfunctions in transient swing of temperature around threshold. Notice is written in p.34.

・Power Good Circuit(PG)

PG is a NMOS open drain form terminal and when SCP is detected, inner NMOS FET turns on and pull-down with 350Ω(typ.) Refer to p.11,12 about PG operation.

・CH1,2 Softstart Good Circuit(CH1G,CH2G)

CH1G, CH2G is inverter output form terminals power supply of them is VREGA and they detect finish of softstart of CH1 and CH2. When CTL terminal of each channel is L or while output voltage is lower than 90% of setting output voltage after CTL terminals are turned on, the output of these terminals is L. And at the end of softstart, when output voltage becomes greater than 90% of setting output voltage, the output voltage of CH1,2G terminal turns to H.(As shown in Figure. 57, CH1G output turns to L when CTL1 is turned off, but while CH1 is in the stop delay time, output of CH1 continues.) Note that the output of CH1,2G terminals is kept H when output voltage drops below 90% of setting output voltage after softstart finished. Startup sequence of each channel can be controlled by connecting CH1,2G terminals to CTL terminals of other channels. Refer to p.30 about timing chart of CH1,2 softstart good function.

・Light Load Mode Control Circuit(SEL)

Control mode of CH2 and 4 is selected between PWM mode and light load mode by SEL terminal. When voltage of SEL terminal is over 2.5V and less than VCC voltage, light load mode is enabled. And when the terminal is open or voltage of that is over -0.3V and less than 0.8V, it is disabled. SEL terminal contains pull-down resistor of 400kΩ (typ.) When you use this function, we recommend to short SEL terminal to VREGA.

・Over Current Protection Circuit(OCP)

OCP prevents destruction of IC from over current flow through internal FET in overload situation or output shorted to GND by detecting input current. When OCP is detected, output switching duty is down to minimum duty, and thus, input current is limited and output voltage decrease. Finally, SCP operates and all DC/DC output stops safely. Refer to p.4 about detect current limit. About CH3, OCP is detected when output current becomes greater than 1.8A under the conditions of VO3 output voltage setting is 5.0V.

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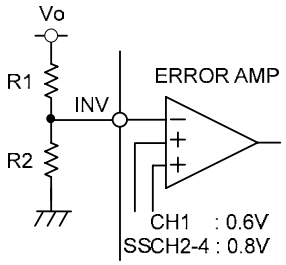
●peripheral components setting

・Setting the switching frequency

The switching frequency FOSC is set by the resistor connected to RT terminal. Connect 82kΩ to set to 1.0MHz.
Switching frequency is calculated as below. Confirm the frequency with IC after select RT value with this equation.

$$Fosc = \frac{82}{R_{RT}} \times 1000[kHz]$$

・Setting output voltages



$$Vo = \frac{(R1+R2)}{R2} \times 0.6[V] \cdots (1)$$

$$Vo = \frac{(R1+R2)}{R2} \times 0.8[V] \cdots (2)$$

Figure.52 Setting output voltages

Output voltages of each channel are determined by feedback resistor R1 and R2 as equation (1) for CH1 and (2) for CH2 to 4.
This IC contains phase compensation, so choose sum of R1 and R2 value between 90kΩ to 1MΩ for CH1 and CH2, 100kΩ to 500kΩ for CH3 and 70kΩ to 300kΩ for CH4, and sufficiently confirm there is no abnormal oscillations.

・Terminal manipulate method for not used channel

Set each terminal of the channel as below when you don't use.

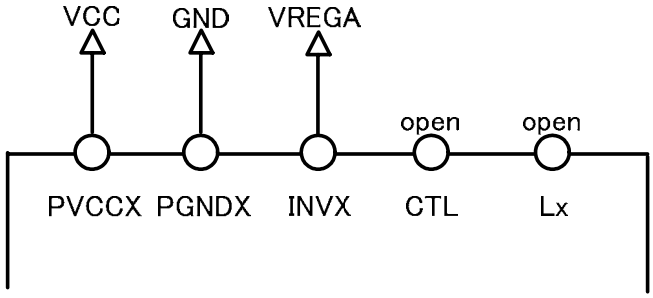


Figure.53 Terminal manipulate method for not used channel

・Setting of SCP timer

Monitoring the output voltages of error amplifier (EOUT voltage), if the voltages become over 3.0V(typ.), the output of SCPCOMP turns to L, and transistor Q1 will turn off. Thus the current of 5uA is supplied to Cscp. DC/DC outputs stop when voltage of Cscp reaches to the threshold voltage (Vtsc≒0.5V). The time from short circuit detection to outputs stop is determined as below.

$$T_{SCP}\ [sec] \fallingdotseq \frac{0.5[V] \times C_{SCP}[\mu F]}{5.0[\mu F]}$$

To reset from SCP latch state, turn CTL to L.
Refer to p.11, 12 about SCP operating timing chart.

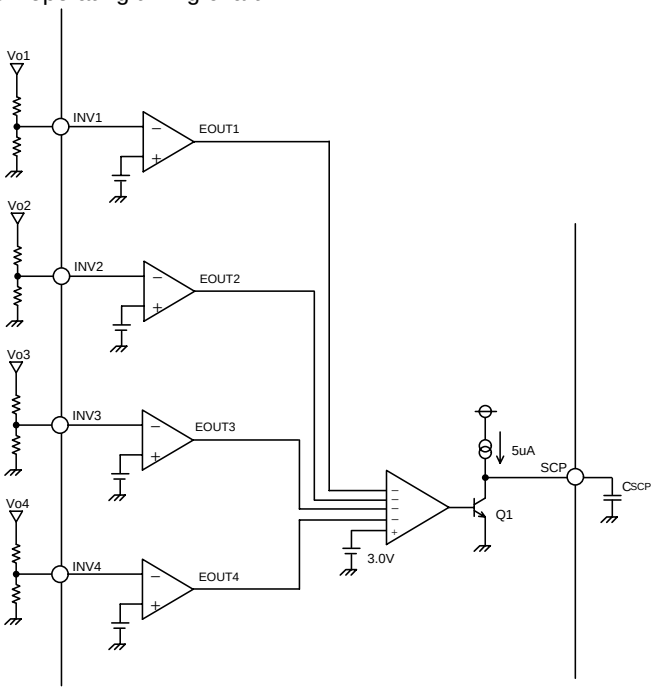


Figure.54 Short Circuit Protection

・About output voltage setting of CH1,2 and 4

The switching duty of CH1, 2 and 4 can reach to 100% but they have maximum duty cycle between 90 to 95%. Thus, when voltage difference between input and output is small or load current is large under the condition of SCP is enabled, SCP may operate. Normally, switching ON Duty of buck converter is calculated as VOUT / VIN, but in fact, it is VOUT / (VIN-Io×Ron) with there is load current. When switching duty become above maximum duty, the output switching turns to 100% duty, but the state of 100% duty output is only allowed transiently before SCP operates. So, set output duty not to exceed the maximum duty cycle.

・Selection of inductor

We recommend the ones of those current rating is sufficiently larger than the peak current value Ipeak written as below and DCR is small and shield type.
The inductor value has much influence to the ripple current.
As shown in the equation below, the larger the inductor value is or higher the switching frequency is, the smaller ripple current becomes

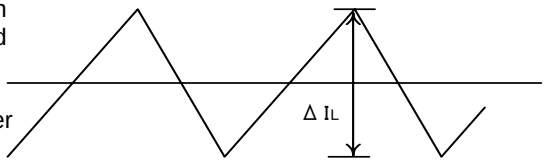


Figure.55 ripple current of inductor

$$Ipeak = Iout + \frac{\Delta IL}{2}\ [A] \cdots\cdots \text{buck converter mode(1)}$$

$$Ipeak = Iout \times \frac{Vin + Vout}{2 \times 0.8 \times Vin \times \eta} + \frac{\Delta IL}{2}\ [A] \cdots\cdots \text{buck/boost converter mode(2)}$$

$$Ipeak = Iout \times \frac{Vout}{Vin \times \eta} + \frac{\Delta IL}{2}\ [A] \cdots\cdots \text{boost converter mode(3)}$$

$$\Delta IL = \frac{(Vin - Vout)}{L} \times \frac{Vout}{Vin} \times \frac{1}{f}\ [A] \cdots\cdots \text{buck converter mode(4)}$$

$$\Delta IL = \frac{|(Vin - Vout)|}{L} \times \frac{Vout \times 2 \times 0.8}{(Vin + Vout)} \times \frac{1}{f}\ [A] \cdots\cdots \text{buck/boost converter mode(5)}$$

$$\Delta IL = \frac{(Vout - Vin)}{L} \times \frac{Vin}{Vout} \times \frac{1}{f}\ [A] \cdots\cdots \text{boost converter mode(6)}$$

(η : power conversion efficiency, ΔIL : ripple current, f : switching frequency)

Generally, choose inductance value as that the ripple current is within 20% to 50% of the output maximum current.
If the inductor current exceeds the maximum rating current of the inductor, a saturation of inductor occurs and may cause an abnormal degradation of efficiency or oscillation. So, choose inductor value with sufficient margin not to peak current exceeds maximum rating current of the inductor.

・Selection of output capacitor

We recommend a low ESR ceramic capacitor as output capacitor to reduce output ripple voltage. And , under consideration of its DC bias characteristics, choose the ones of those maximum rating voltage is sufficiently higher than output voltage.
The output ripple voltage is calculated as in the equation below with a ceramic capacitor.

$$Vpp = \Delta IL \times \frac{1}{2\pi \times f \times Co} + \Delta IL \times R_{ESR}[V] \cdots\cdots (7)$$

Confirm the ripple voltage with IC after choose the capacitor with this equation to the output ripple voltage is within allowed value.

・Setting of external synchronization

When you use external synchronization function, stop external clock after IC stops. If it is stopped before IC stops, discharge of triangle waveform (slope waveform) is interrupted and the internal oscillator stops, thus, DC/DC stops. Additionally, force power supply voltage of IC before start to input the external clock to SYNC terminal. There is an anti-ESD diode between SYNC terminal and VCC terminal, so, before supply voltage is forced, current flows from SYNC terminal to VCC terminal through the diode.

The external synchronization function, the switching frequency of DC/DC is synchronized with any external clock, works by turning on CTL under the condition of inputting external clock pulse to SYNC terminal.
This IC controls to increase RTSS voltage in order to maintain the top voltage of the internal triangle waveform when external synchronization is used. If the frequency of input clock is out of the possible RTSS voltage range, the IC cannot maintain the height of internal slope waveform, so, set the frequency of input clock within 20% higher than the frequency that is determined by the resistor connected to RT terminal as below..

frequency set by resistor at RT ＜ frequency input to SYNC ＜ (frequency set by resistor at RT x 1.2)

The block of RTSS terminal start with the time constant determined by the capacitor connected to RTSS terminal. To prevent malfunction in startup, internal SS nodes are discharged before RTSS voltage reaches to 0.35V. And also, before RTSS voltage reaches to 0.35V, RTSS output current increase to about 60uA to speed up the startup. The time RTSS voltage reaches to 0.35V is calculated as following equation.

$$T_{RTSS1}[sec] \fallingdotseq \frac{0.35 \times C_{RTSS}[pF]}{60[\mu F]}$$

(ex. T_{RTSS1}≒60µsec @ C_{RTSS}=10000pF)

After RTSS voltage reaches to 0.35V, RTSS output current decrease to 5.0uA, and the time RTSS voltage reached to 0.5V is calculated as following equation..

$$T_{RTSS2}[sec] \fallingdotseq \frac{\{(0.5(*1) - 0.35) \times C_{RTSS}[pF]\}}{5.0[\mu A]}$$

(*1)when the frequency set by resistor at RT nearly equals to external synchronous frequency.

(ex. T_{RTSS2}≒300µsec @ C_{RTSS}=10000pF)

RTSS voltage is maintained by turning current sink and source repeatedly, and switch of current flow is controlled by rise edge of external clock, so, if the capacitor value connected to RTSS terminal is too small,(especially switching frequency is low) the range of voltage swing from one clock to the next may increase. And that may cause inaccuracy of, for example, maximum duty. We recommend around 10000pF when switching frequency is around 1MHz. Note that if you select a larger value than that, stability will increase but the time before output softstart lengthens.

・CH1, 2 Softstart Good function

CH1 and CH2 have softstart good function that detects the finish of softstart of each channel, and CH1G terminal and CH2G terminal are output terminal of each. When CTL terminal of each channel is off or while output voltage is lower than 90% of setting output voltage after CTL terminals are turned on, the output of these terminals is L. And at the end of softstart, when output voltage becomes greater than 90% of setting output voltage, the output voltage of CH1,2G terminal turns to H. As shown in Figure. 56 below, we can control the start up order of each channel by connecting CH1G or CH2G terminal to CTL terminal of other channels. If you connect CH1G terminal to CTL2 and CTL4, after softstart of CH1 finish, CTL2 and CTL4 turn to H and CH2 and 4 start. After that, CH2 finish its softstart, and thus, CTL3 it is connected to CH2G become H and CH3 start operating. In the off sequence, if you turn CTL1 off, all channels will stop (Figure.57)

When you don't use CH1,2 softstart good function, make CH1G, CH2G terminal opened.

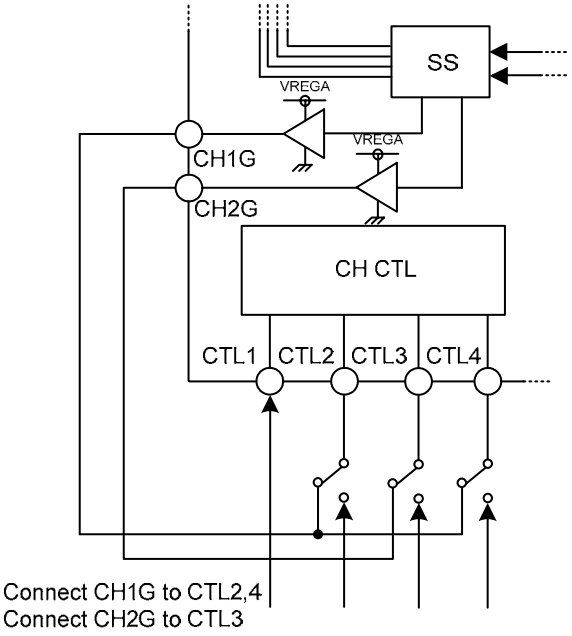


Figure.56 example of startup sequence control

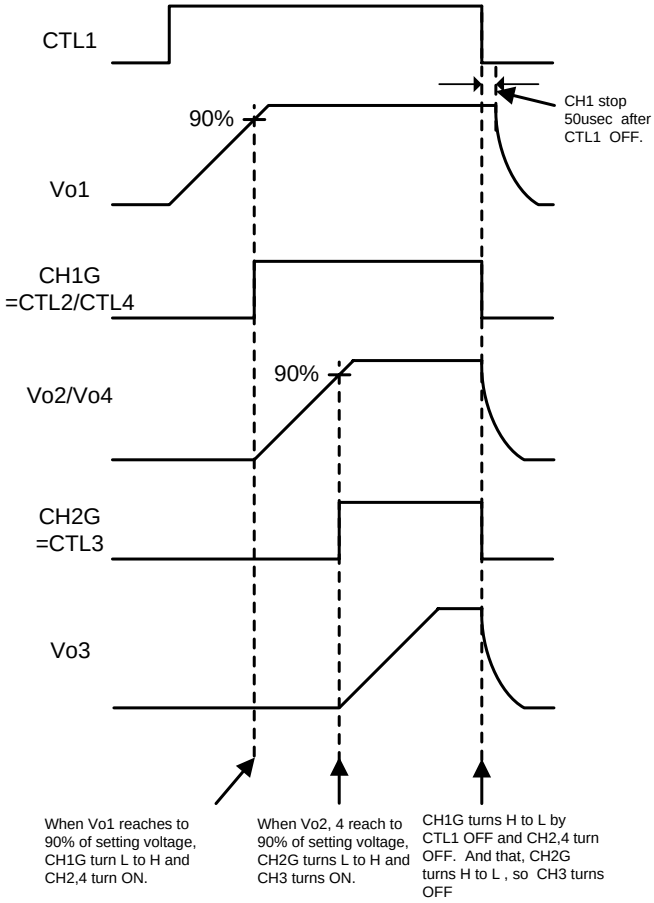


Figure.57 timing chart of startup sequence control

●PCB layout considerations

・Connect input capacitor(bypass capacitor : Cin_bp) to PVCC and PGND through shortest line.

→Its aim is to shorten the current loop and reduce parasitic impedance. Switching current is supplied from power supply Vin(Cin), but there are parasitic impedance or inductance in capacitors or boards, so current supply from bypass capacitor put near the IC when current flow is rapidly changed.

It is a desirable constitution that a large capacitance electrolytic capacitor is used as Cin and a ceramic capacitor is used as a bypass capacitor.

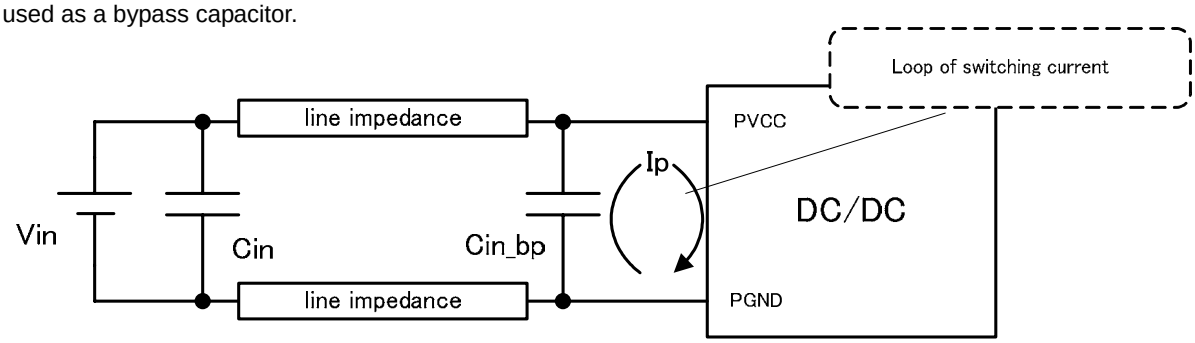
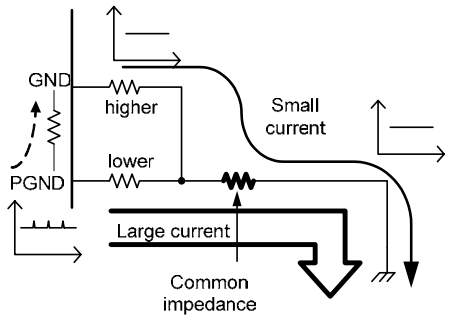


Figure.58 effect of input capacitor

・Layout GND and PGND line wide and short as possible.

→In this IC, subcontact is connected GND and PGND. Because of this, if you separate GND and PGND, and connect them at one point, GND and PGND are connected inside of IC through subcontact. And if inner impedance is lower than impedance of outer connection, the current of PGND terminal flows down to GND terminal. This may have an effect on internal bandgap voltage or oscillator and so on. So,it is needed to reduce outer impedance of PGND line lower than inner impedance of GND line and layout ,GND and PGND line wide and short.



To reduce inner current flow to GND, make the impedance between PGND and PCB ground connect point lower than the inner impedance between GND and PGND. And it is more
effective to increase the outer impedance between GND and PGND.

Figure.59 effect of common impedance

・To avoid interference, layout between feedback resistor and feedback terminals short as possible. An interference of noise to feedback terminals(INV1-4) may cause output abnormal oscillation.

→An interference of noise to feedback terminals(INV1-4) may cause output abnormal oscillation.

・Terminal voltage of VCC and PVCC not exceed absolute maximum ratings.

→If input capacitor are placed far from IC, parasitic inductance of PCB may cause ringing and the terminal voltage exceed the absolute maximum ratings. For reference, place input capacitor within 5.0mm from IC under the condition of that, thickness of PCB pattern is 35um, width of it is 1.0mm.

●Pin equivalent circuit

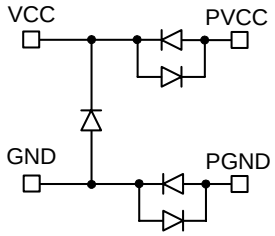
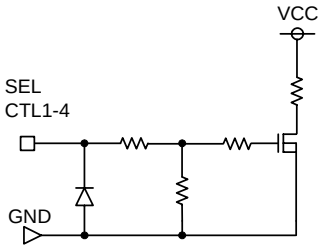
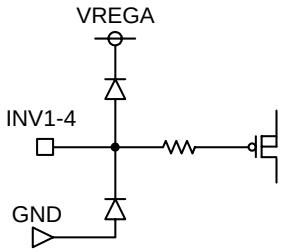
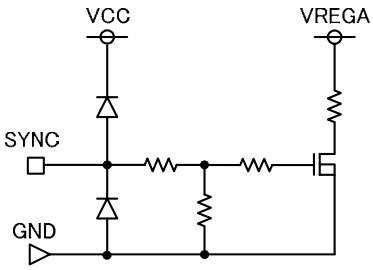
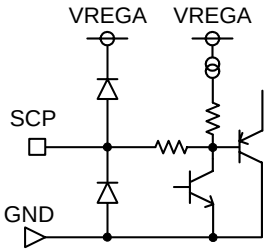
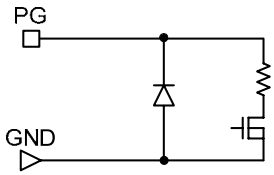
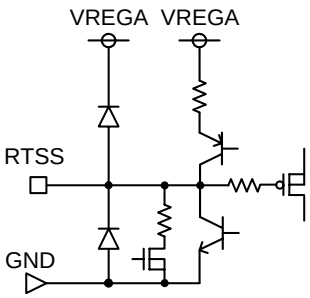
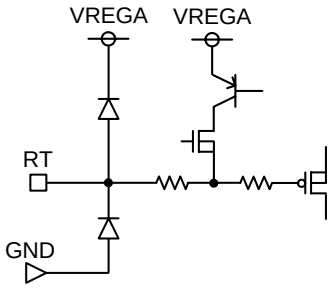
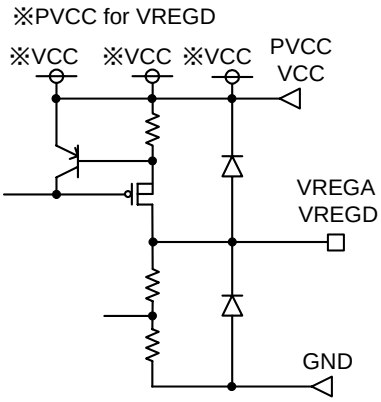
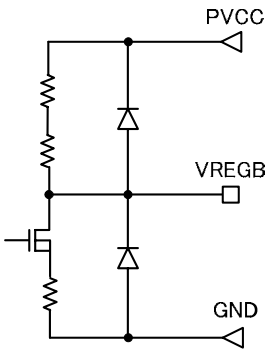
	Name	Pin equivalent circuit			Name	Pin equivalent circuit
G6 G5 G4 B3	VCC GND PVCC PGND			C4 D3 C6 C5 C7	CTL1 CTL2 CTL3 CTL4 SEL	
F3 D4 E4 E5	INV1 INV2 INV3 INV4			E3	SYNC	
B4	SCP			B5	PG	
D5	RTSS			F6	RT	
F5 G3	VREGA VREGD			F4	VREGB	

Figure.60 Pin equivalent circuit 1

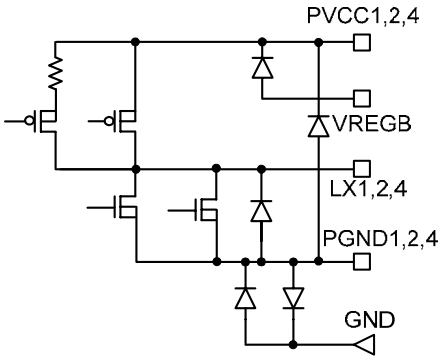
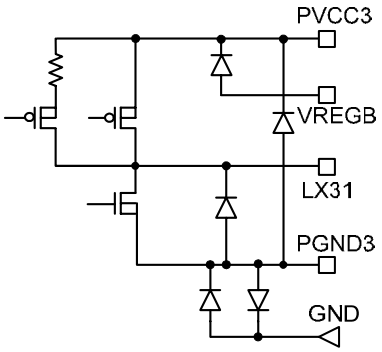
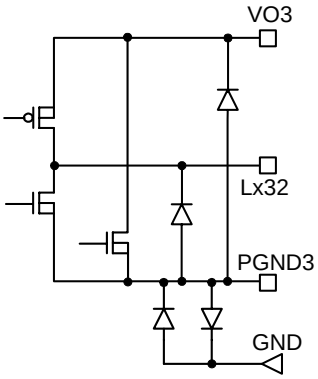
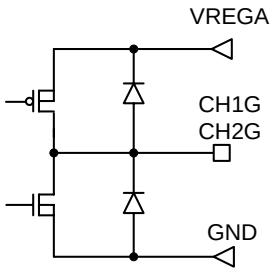
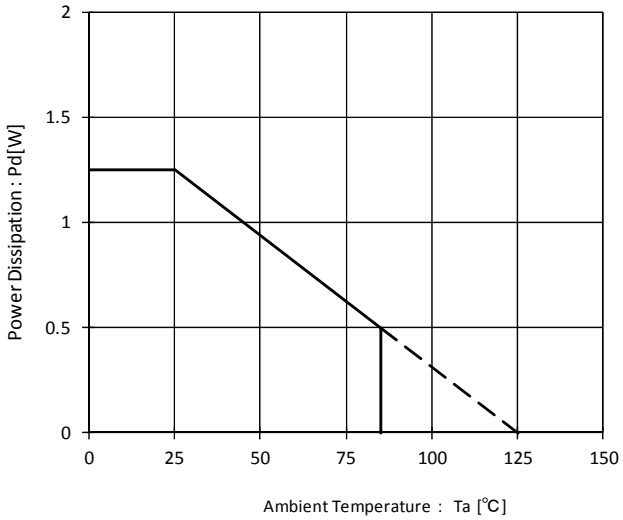
	Name	Pin equivalent circuit			Name	Pin equivalent circuit
G1,G2 A1,A2 F7,G7 F4 E1,F1 B1,B2 E6,E7 D1,D2 C1,C2 D6,D7	PVCC1 PVCC2 PVCC4 VREGB Lx1 Lx2 Lx4 PGND1 PGND2 PGND4			A3 F4 A4 A5,A6	PVCC3 VREGB Lx31 PGND3	
B7 A7,B6 A5,A6	VO3 Lx32 PGND3			F2 E2	CH1G CH2G	

Figure.61 Pin equivalent circuit 2

●Thermal Derating Curves



When mounted on a 50mm × 50mm × 1.75mm glass epoxy 8layers PCB.
Should be derated by 12.5mW/℃ Ta=25℃ or more.
Heat design should consider tolerance dissipation during actual use and margins which should be set plenty of room.

Figure.62 Power dissipation

●Usage Notes

1.) Absolute maximum ratings
This product is produced with strict quality control. However, the IC may be destroyed if operated beyond its absolute maximum ratings. If the device is destroyed by exceeding the recommended maximum ratings, the failure mode will be difficult to determine. (E.g. short mode, open mode.) Therefore, physical protection counter-measures (like fuse) should be implemented when operating conditions beyond the absolute maximum ratings anticipated.

2.) GND potential
Make sure GND is connected at lowest potential. All pins must not have voltage below GND.

3.) Thermal design
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4.) Pin shorts and mounting errors
Use caution direction and position the IC for mounting on printed circuit boards. Improper mounting may result in damage the IC. In addition, Output-output short and output-power supply/ground short condition may destroy the IC.

5.) Actions in strong magnetic field
Exposing the IC within a strong magnetic field are may cause malfunction.

6.) Common impedance
Power supply and ground wiring should reflect consideration of the need to lower common impedance and minimize ripple as much as possible. (by making wiring as short and wide as possible or rejecting ripple by incorporating inductance and capacitance.)

7.) Thermal shutdown circuit (TSD circuit)
This IC incorporates a built-in thermal shutdown circuit (TSD circuit.) The TSD circuit is designed only to shut the IC off to prevent from thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

8.) Rush current at the time of power supply injection
An IC which has plural power supplies, or CMOS IC could have momentary rush current at the time of power supply injection. Please take care about power supply coupling capacity and width of power supply and GND pattern wiring.

9) Influence by strong light
When large amount of light like strobe is come in, IC can act under wrong operation. Please make light removal system and check operations adequately.

10) IC terminal input
. This IC is a monolithic IC, and between each element there is a P+ isolation and P substrate for element separation. There is a P-N junction formed between this P-layer and each element's N-layer, which makes up various parasitic elements.
For example, when a resistor and a transistor are connected with a terminal as in Figure. 63:
○When GND＞(terminal A) at the resistor, or GND＞(terminal B) at the transistor (NPN), the P-N junction operates as a parasitic diode.
○Also, when GND＞(terminal B) at the transistor, a parasitic NPN transistor operates by the N-layer of other elements close to the aforementioned parasitic diode.

With the IC's configuration, the production of parasitic elements by the relationships of the electrical potentials is inevitable. The operation of the parasitic elements can also interfere with the circuit operation, leading to malfunction and even destruction.
Therefore, uses which cause the parasitic elements to operate, such as applying voltage to the input terminal which is lower than the GND (P-substrate), should be avoided.

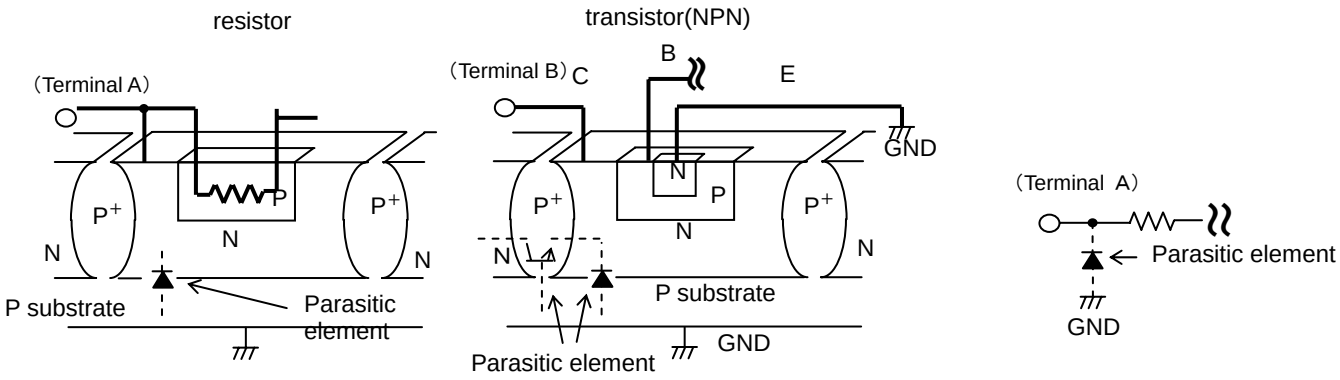


Figure. 63 Simplified structure of bipolar IC

●Ordering Information

B	D	9	8	6	6	G	U	L	E 2

Part Number

Package
GUL:VCSP50L3

Packaging and forming specification
E2:Embossed tape and reel

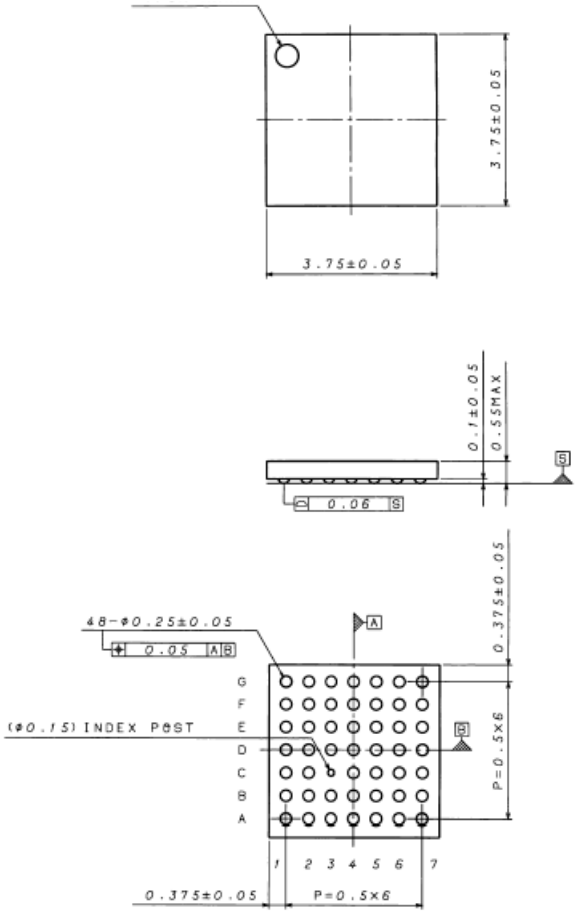


Figure. 64 Package dimensions (UNIT:mm)

Tape	Embossed carrier tape
Quantity	2,500pcs / Reel
Direction of feed	E2

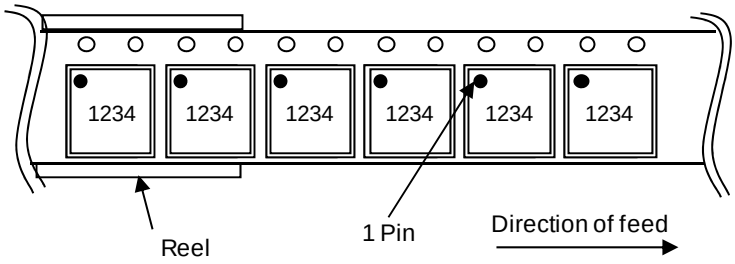


Figure. 65 Direction of feed

●Marking Diagram

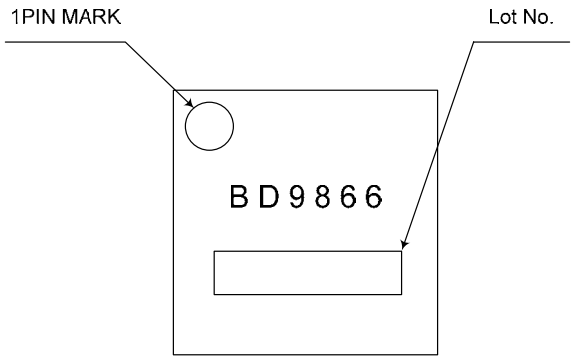


Figure. 65 Marking diagram

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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